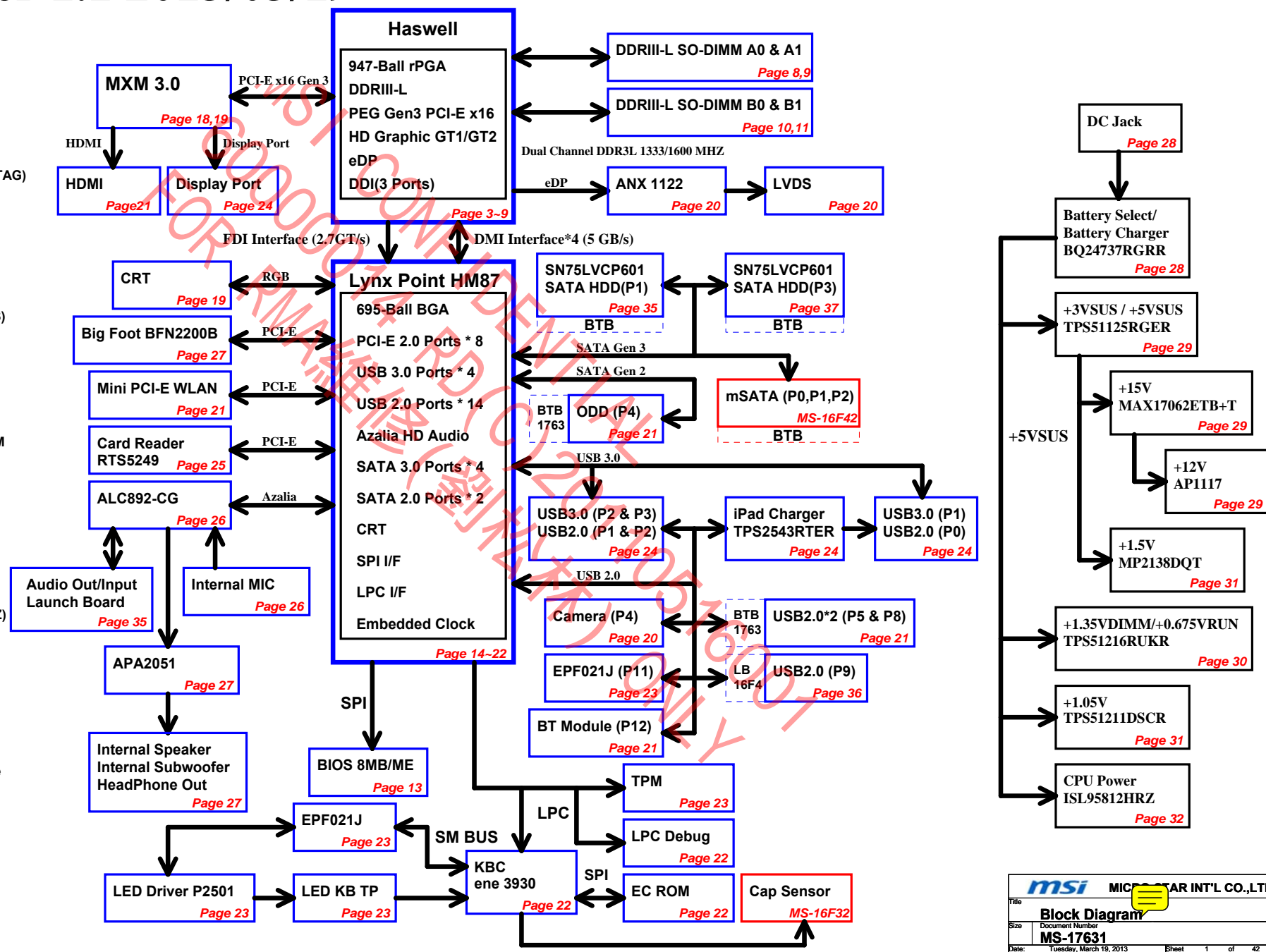


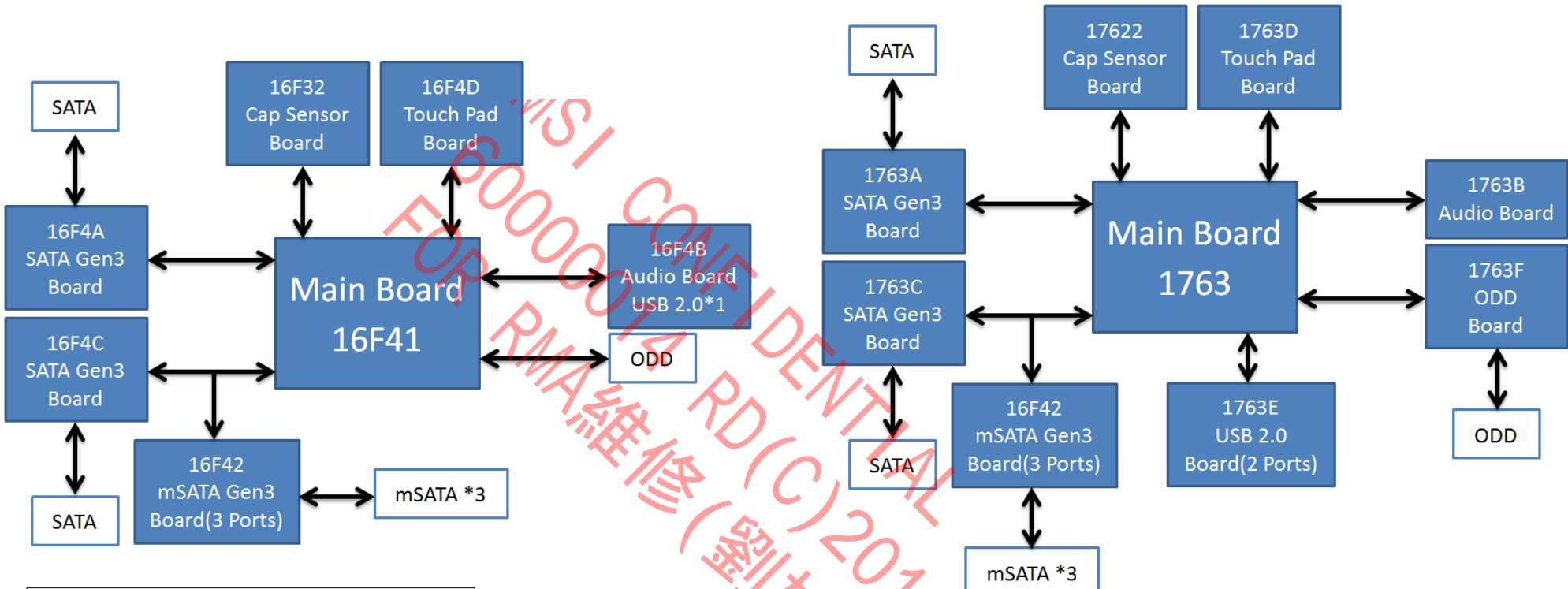
Shark Bay Platform

MS-1763 Ver 1.1 2013/03/19

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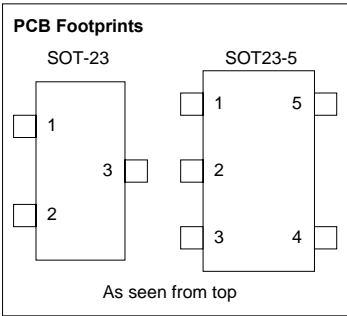
Board Diagram



Voltage Rails			
Power Plane	Voltage	Active In	Description
PWR_SRC	19V or 12 V	S0, S3-S5	Power Source
+5VALW	5V	S0, S3-S5	
+3VALW	3.3V	S0, S3-S5	
+5VSUS	5V	S0, S3	
+3VSUS	3.3V	S0, S3	
+1_35VDIMM	1.35V	S0, S3	DDR3L Power
+5VRUN	5V	S0	
+3VRUN	3.3V	S0	
+1_5VRUN	1.5V	S0	PCH Power for I/O
+12V_FAN	12V	S0	Fan Power
+15V	15V	S0	LED Keyboard Power
+0_675VRUN	0.675V	S0	
+1_05VRUN	1.05V	S0	
+VCC_CORE	1.2V	S0	Processor Core Power Rail

Net Naming Conventions
Suffix
= Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

Power States						
	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+V*SUS	+V*RUN
S0 (Full on)	High	High	High	On	On	On
S3 (Suspend to RAM)	Low	High	High	On	On	Off
S4 (Suspend to Disk)	Low	Low	High	On	Off	Off
S5 (Soft off)	Low	Low	Low	On	Off	Off

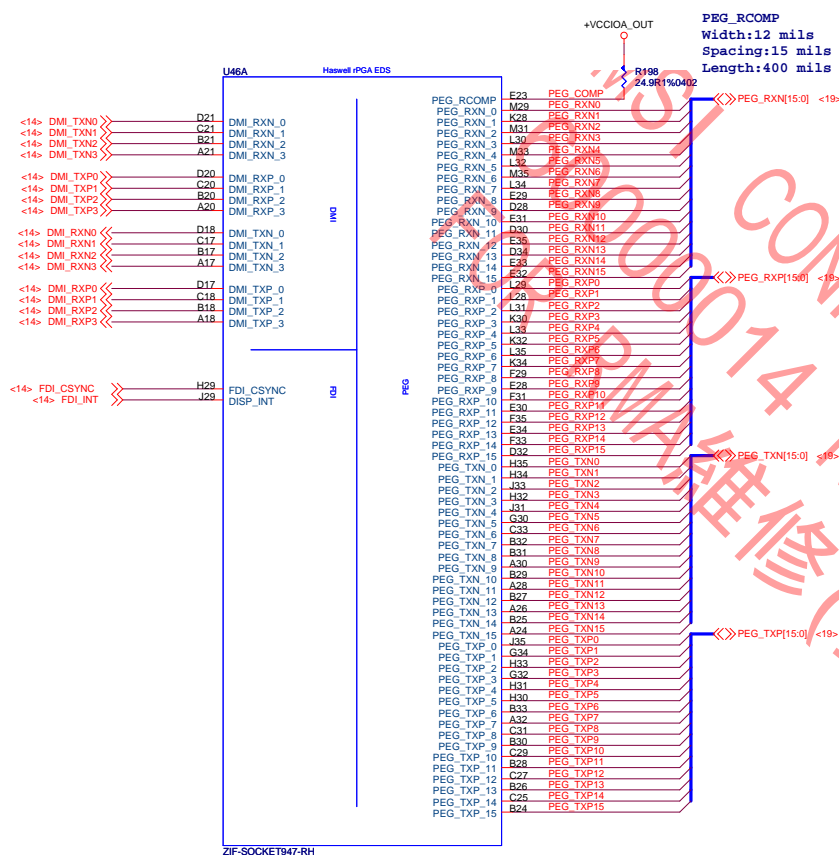
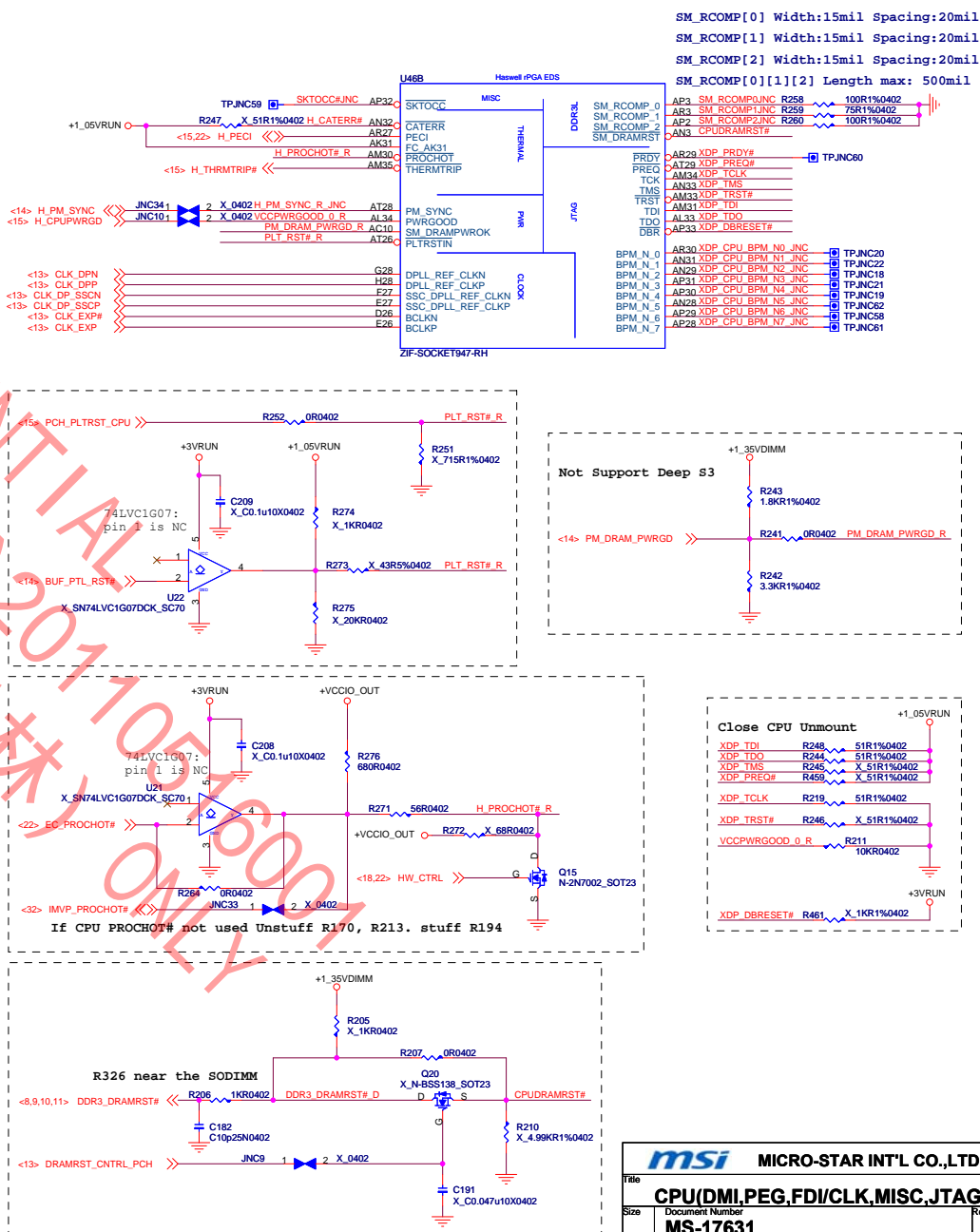


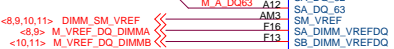
MS-17631 Change List

Date	Page	Description	Date	Page	Description	Date	Page	Description
2012.11.20	14	R335 Unstuff						
	20	Change U30 SDA & SCL Pin						
	25	CardReader Change to RTS 5249						
2013.01.14	18	Modify MXM 5VRUN Power						
	19	Modify MXM GC6						
	20	Modify ANX 1122 SMB Channel						
		Ver. Change to 1.0						
2013.01.21	28	PQ13 & PQ14 Change to D03-0444703-A68						
		Ver. Change to 1.1						
2013.03.19		Remove CPU GAP						

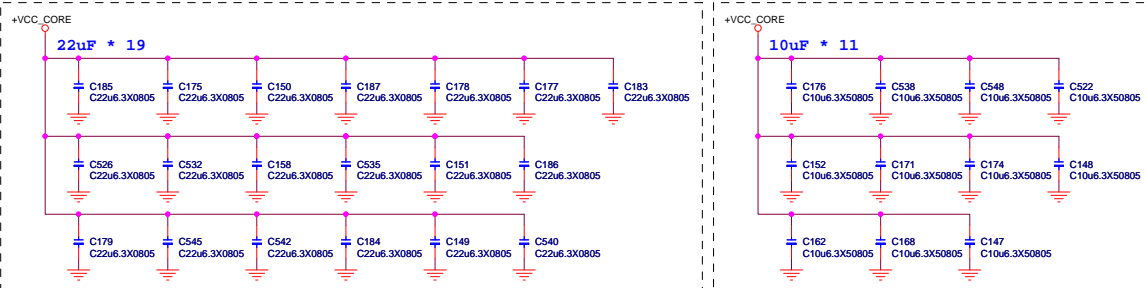
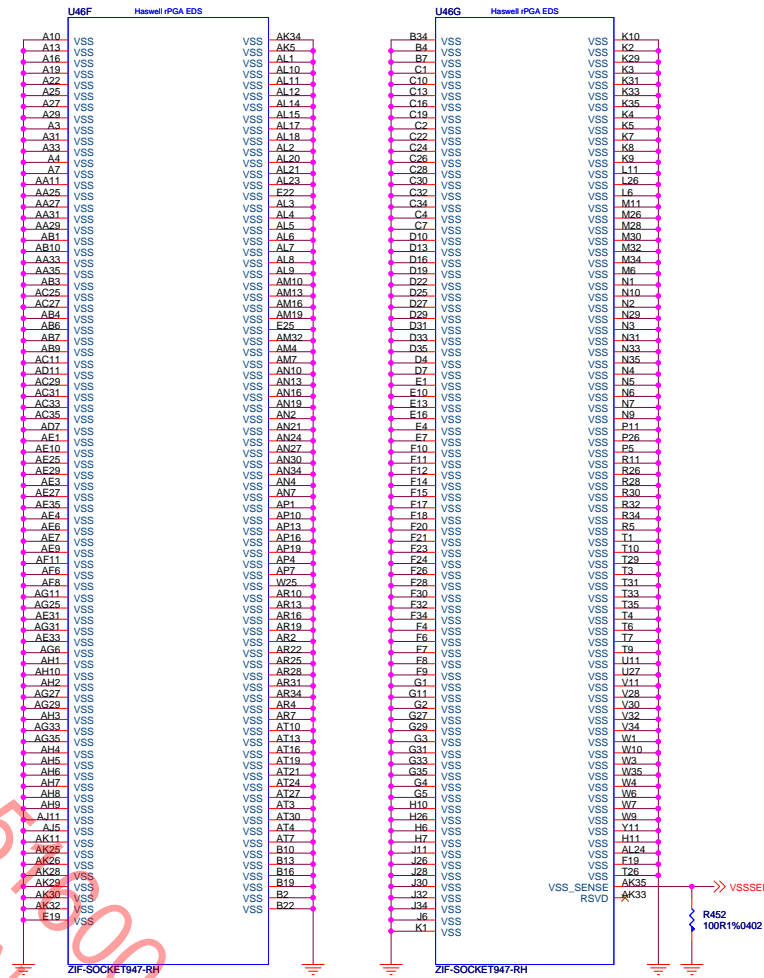
MSI CONFIDENTIAL
60000014 RD(C)20110516001
FOR RMA維修(劉松林) ONLY

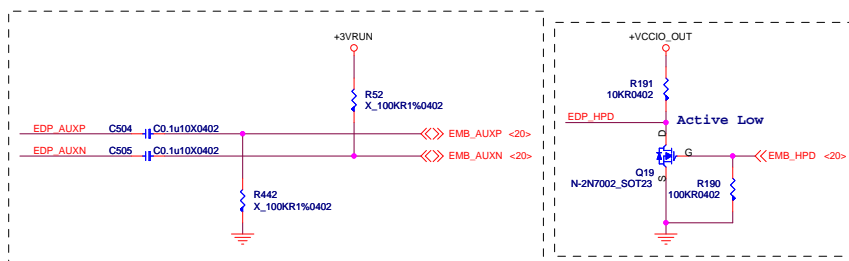
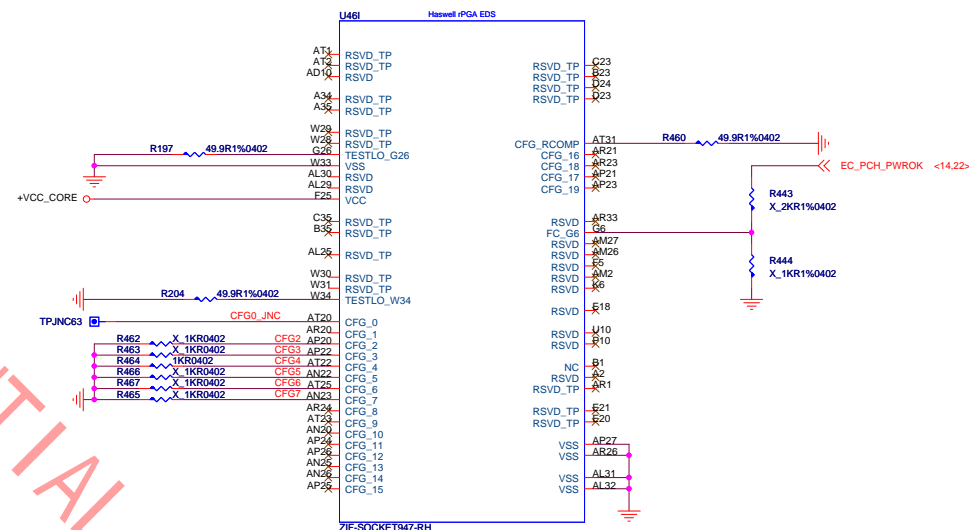
Haswell Processor (DMI,PEG,FDI)

**Haswell Processor (CLK,MISC,JTAG)**

[illegible]

Haswell Processor (Gnd)



Haswell Processor (Reserved)

PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

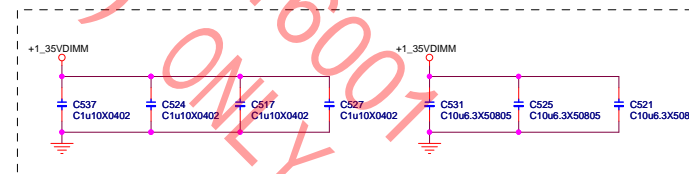
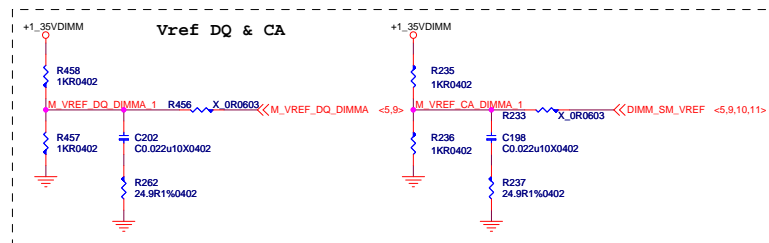
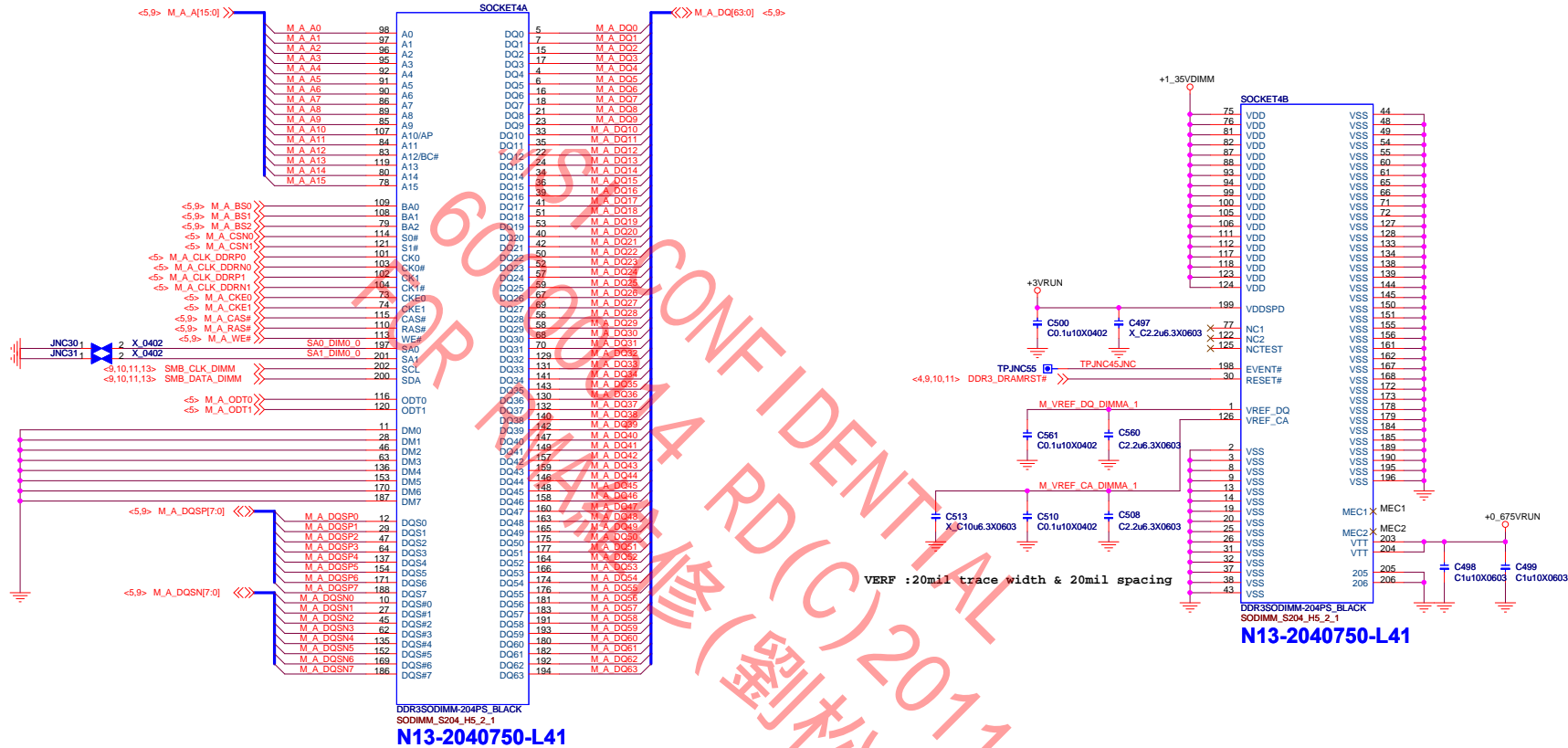
MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP Enable	
CFG4	1 = Disabled 0 = Enabled

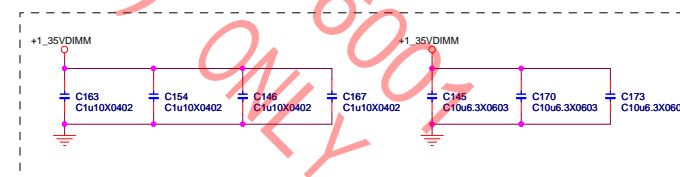
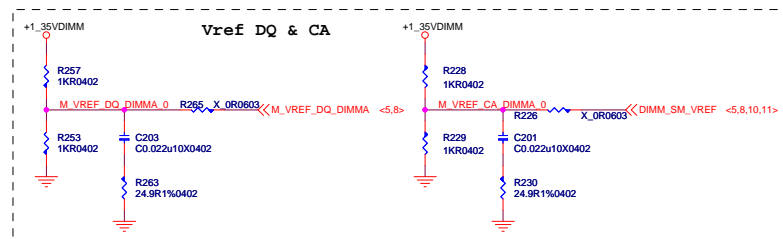
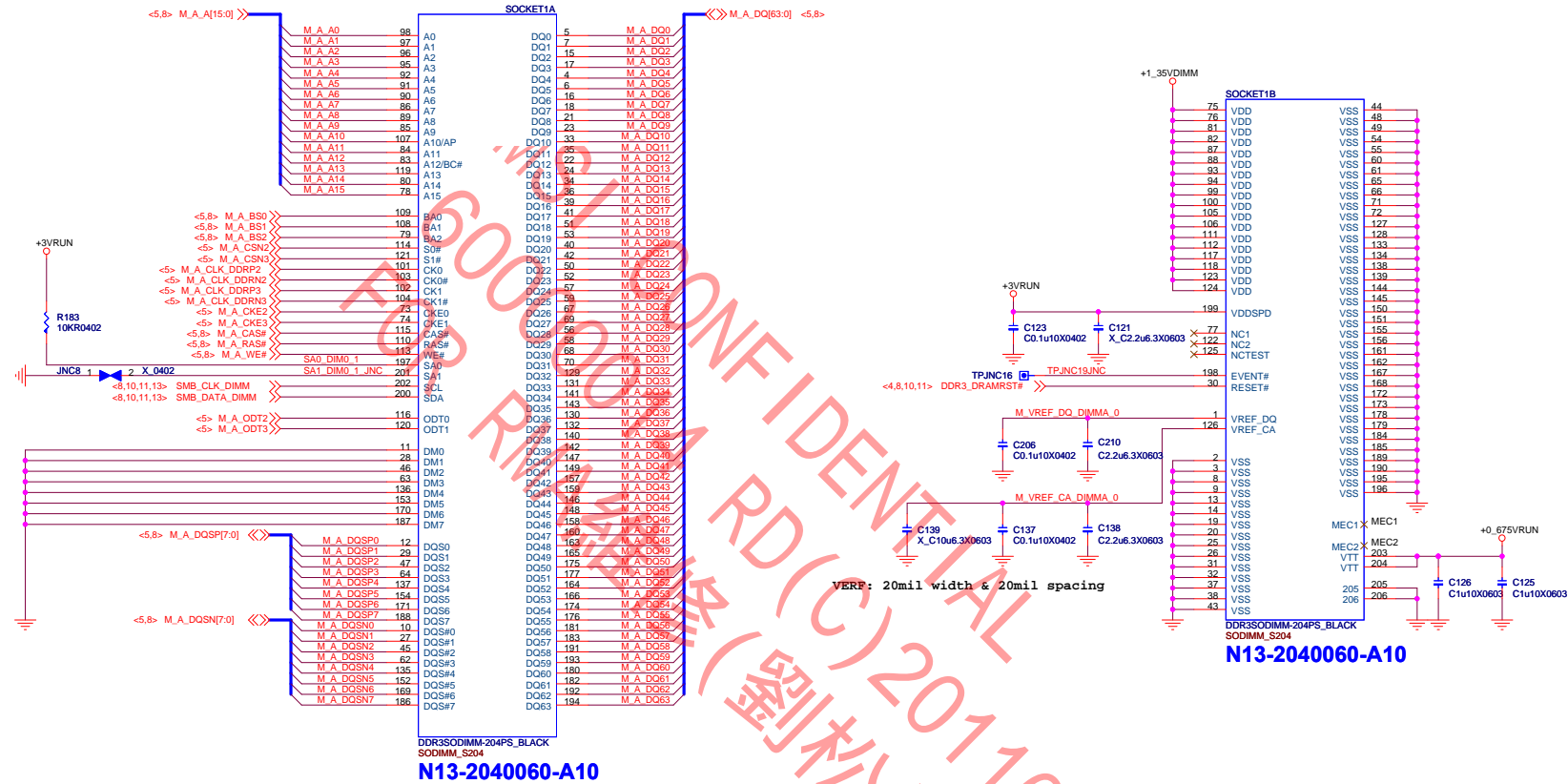
PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express
	01 = reserved
	10 = 2 x8 PCI Express
	11 = 1 x16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

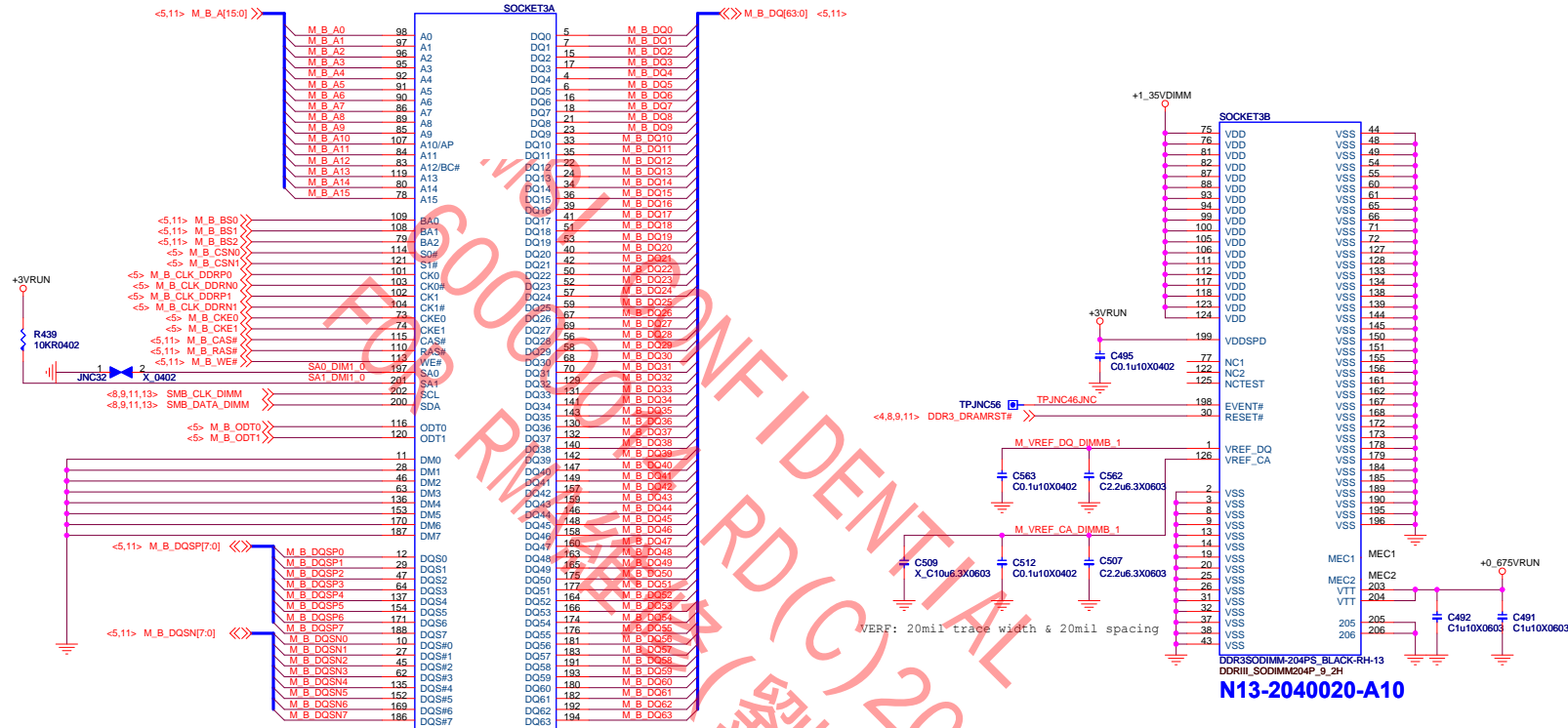
SODIMM #A0



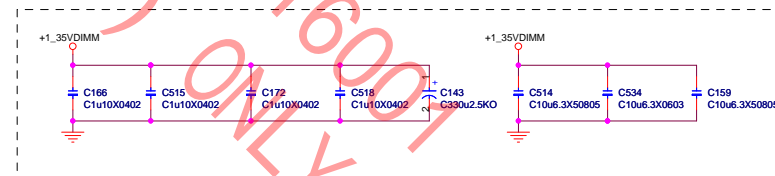
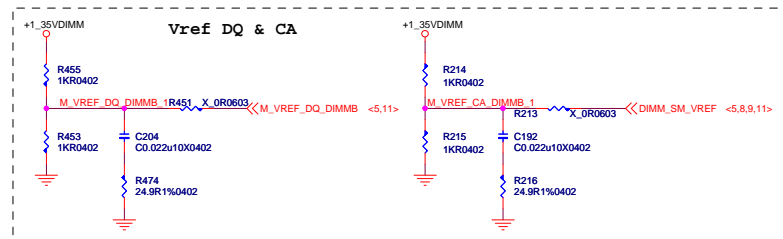
SODIMM #A1



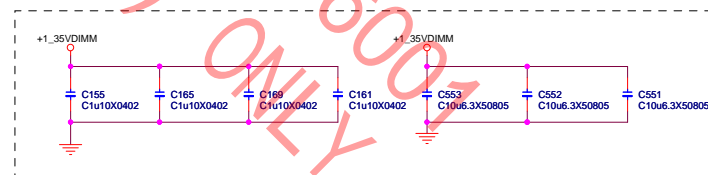
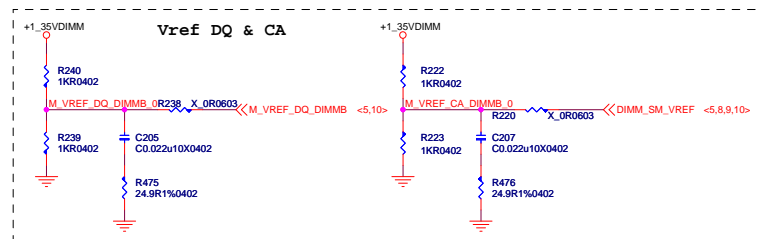
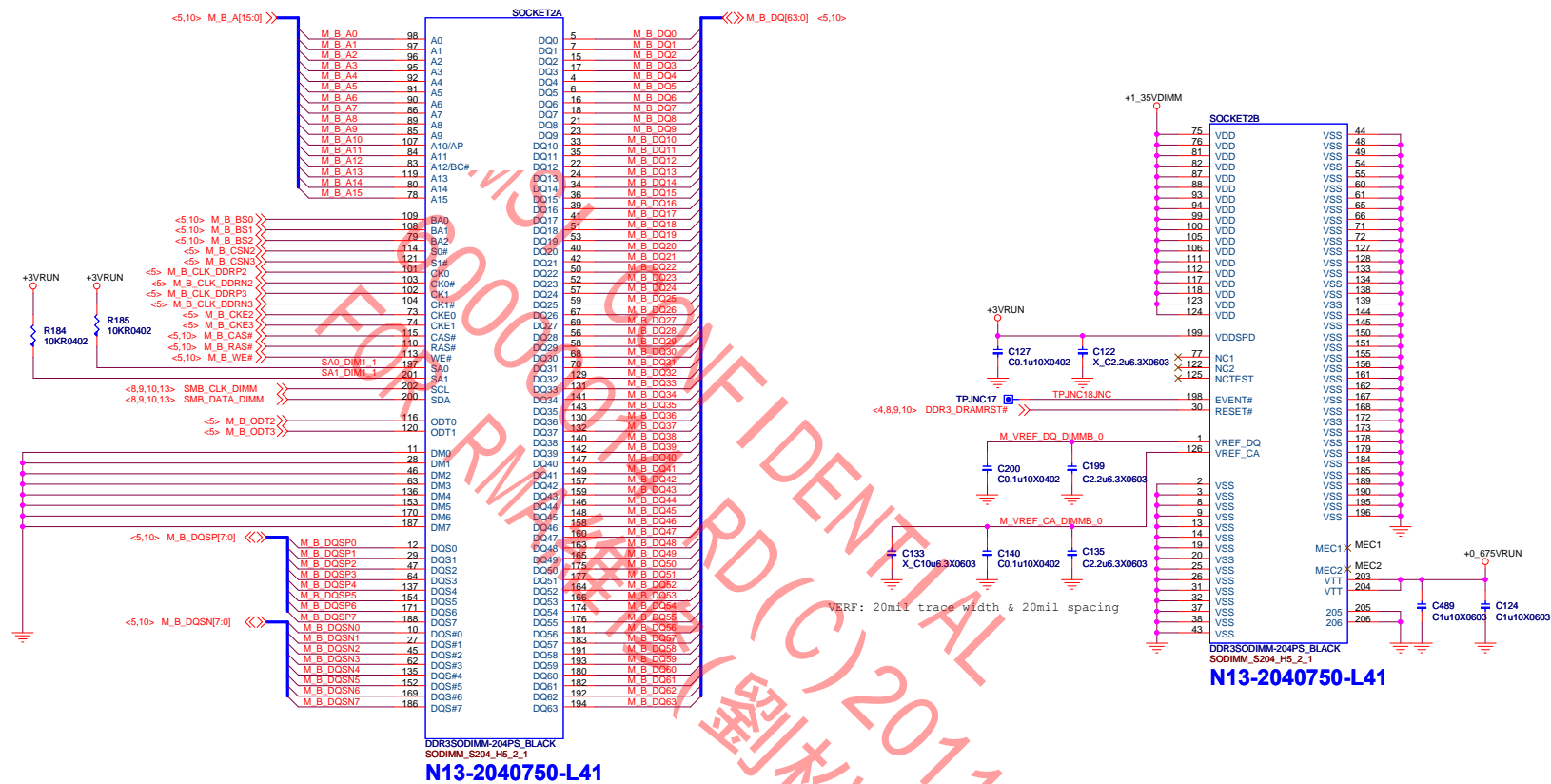
SODIMM #B0



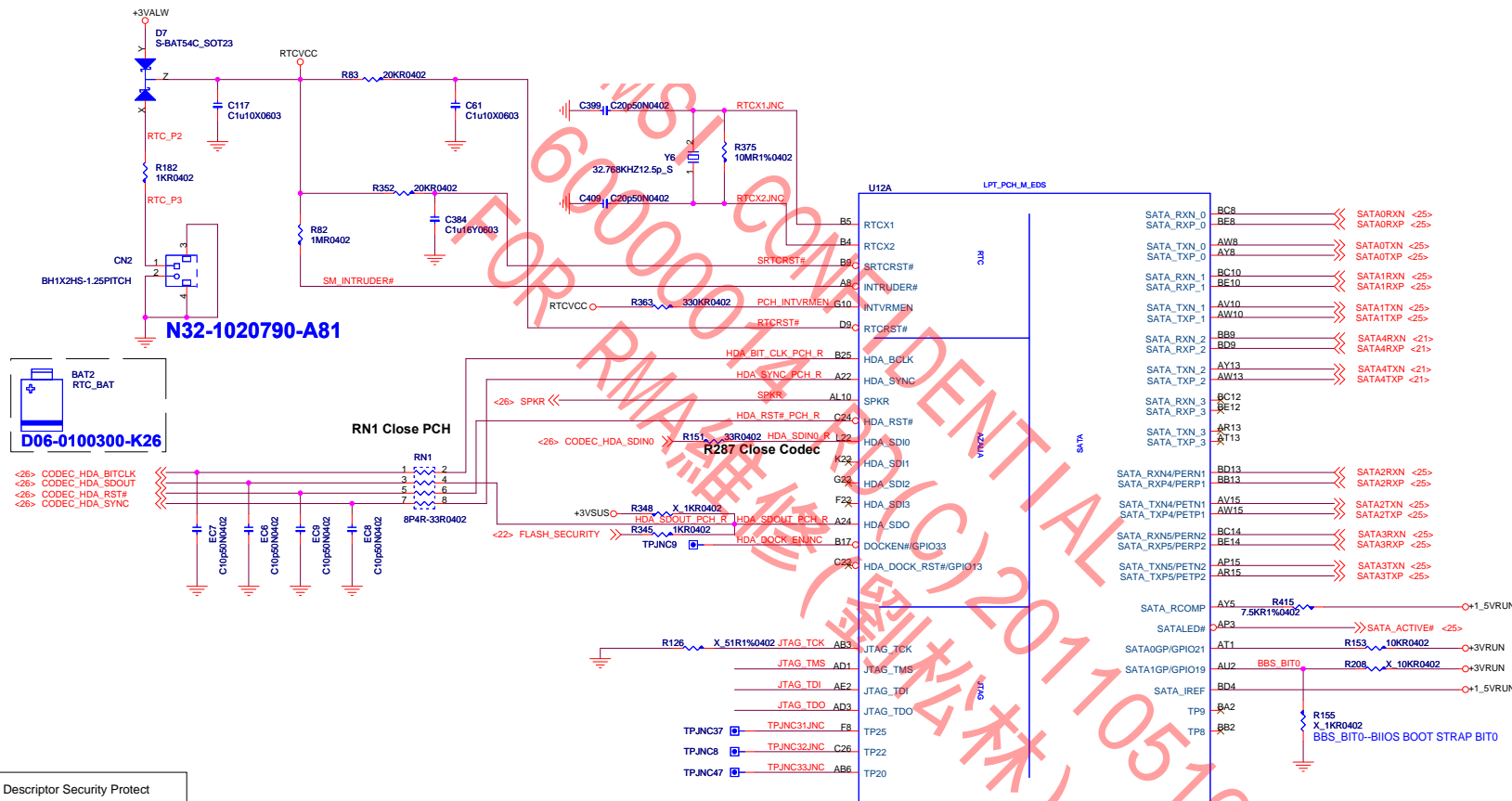
DDR3SODIMM-204PS, BLACK-RH-13
DDR3L_SODIMM204P_9_2H
N13-2040020-A10



SODIMM #B1



Lynx Point (HDA,JTAG,SATA)



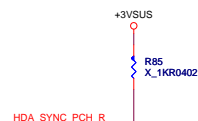
SATA	
Port	Device
0	mSATA Gen3(6Gb/s)
1	mSATA Gen3(6Gb/s)
2	ODD(Gen2)
3	NC
4	mSATA Gen3(6Gb/s)
5	To A board(Gen3)

Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

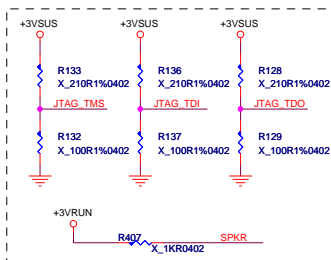
Signal has a weak internal pull-down
Note: The weak internal pull-down is disabled after PLTRST# deasserts.

SPK	<p>The Signal has a weak internal pull-down</p> <p>Note: the internal pull-down is disabled after PLTRST# deasserts.</p> <p>If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)</p>
-----	--

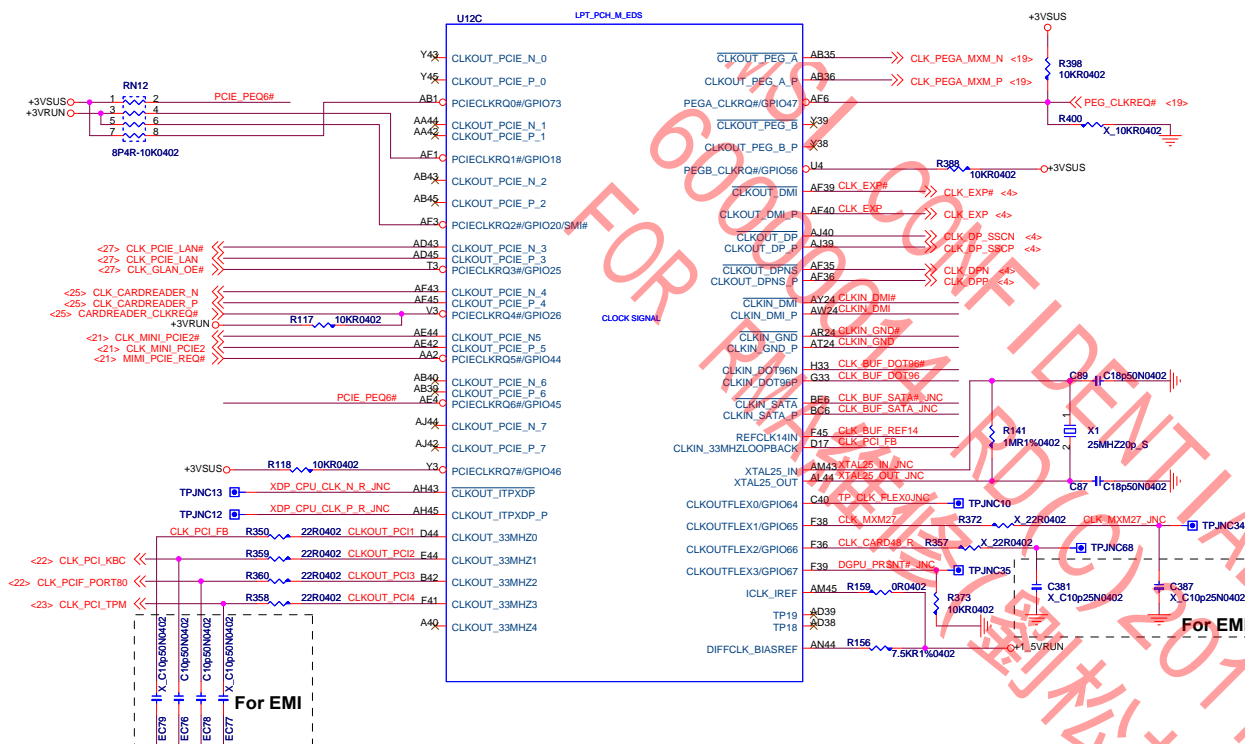
Reserved for Codec use RUN.



HDA_SYNC signal also serves as a strap for selecting VRM voltage to the PCH. The strap is sampled on the rising edge of RSMRST# signal. Due to potential leakage on the codec (path to GND), the strap may not be able to achieve the V_{Imin} at PCH input. Therefore, platform may need to isolate this signal from the codec during the strap phase. The following example circuits maybe used to achieve this purpose.



Lynx Point (Clock)

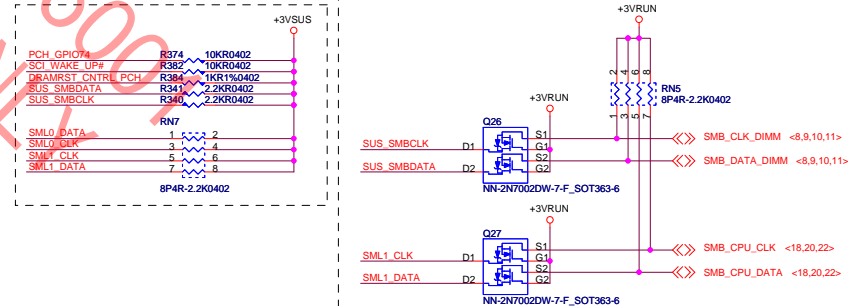
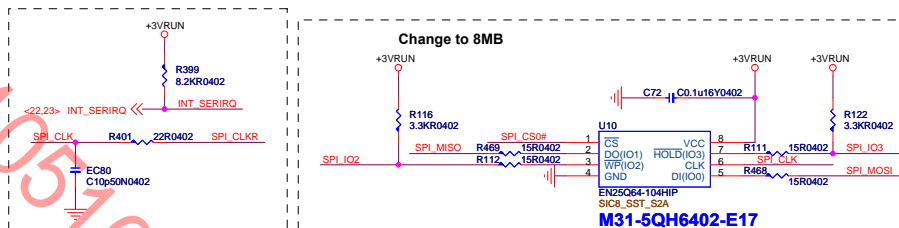
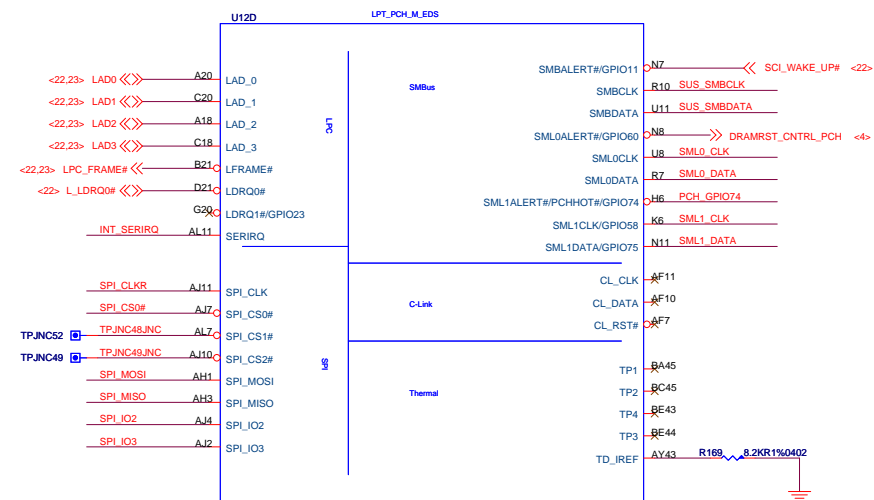


PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKREQ# pin on PCH with 10 k Ω \pm 10% external pull-up resistor instead of No Connect.
Only PCIECLKREQ[2:1]# on PCH are core well powered. All other PCIECLKREQ# are suspend well powered.

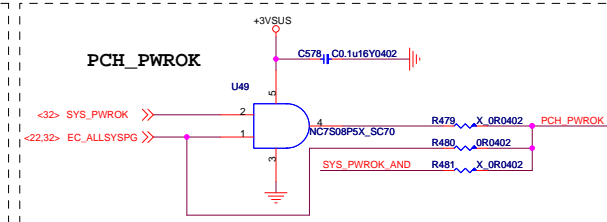
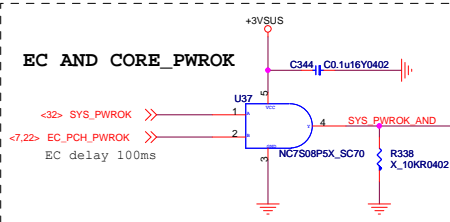
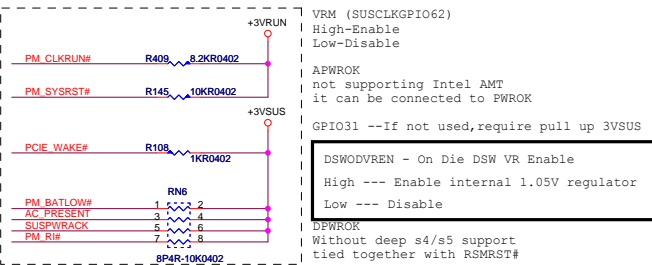
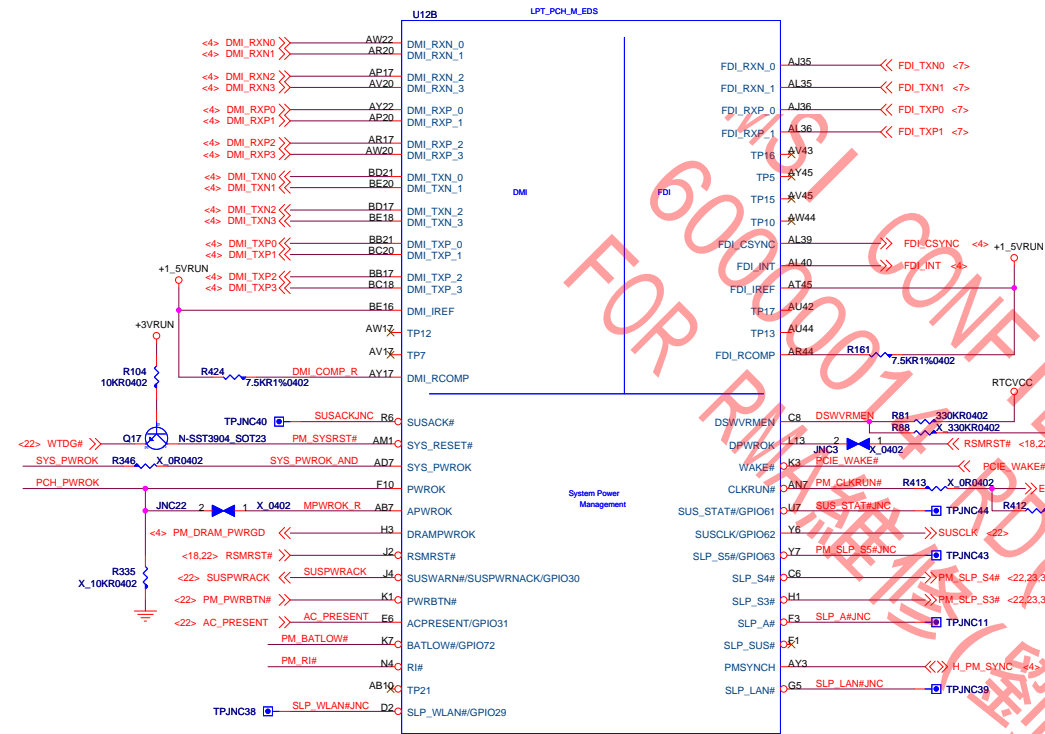
*Disable PCIE OBFF(BIOS)

For Integrated Clock Generation Mode

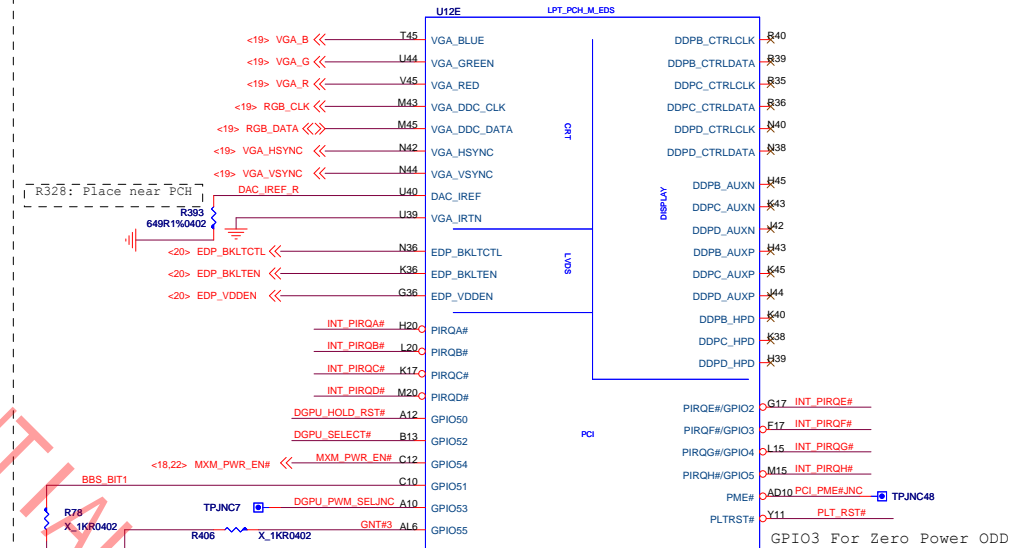
Lynx Point (LPC, SMBUS)



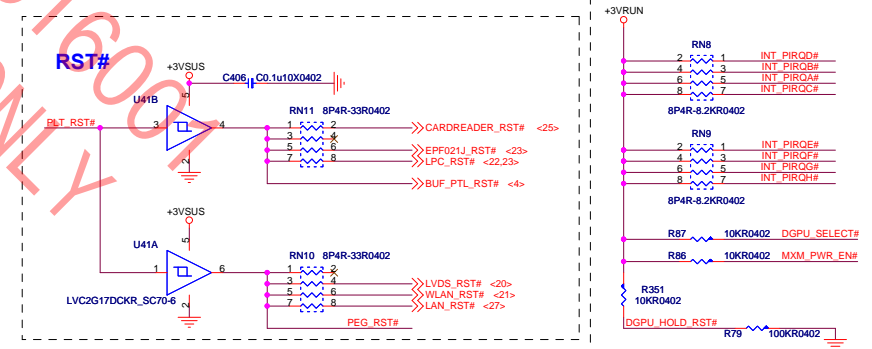
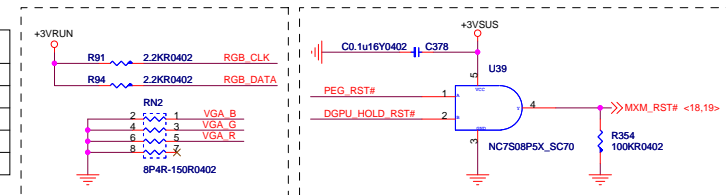
Lynx Point (DMI, FDI)



Lynx Point (PCI, DDI)

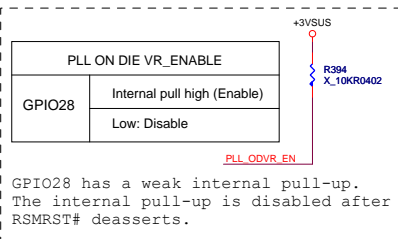
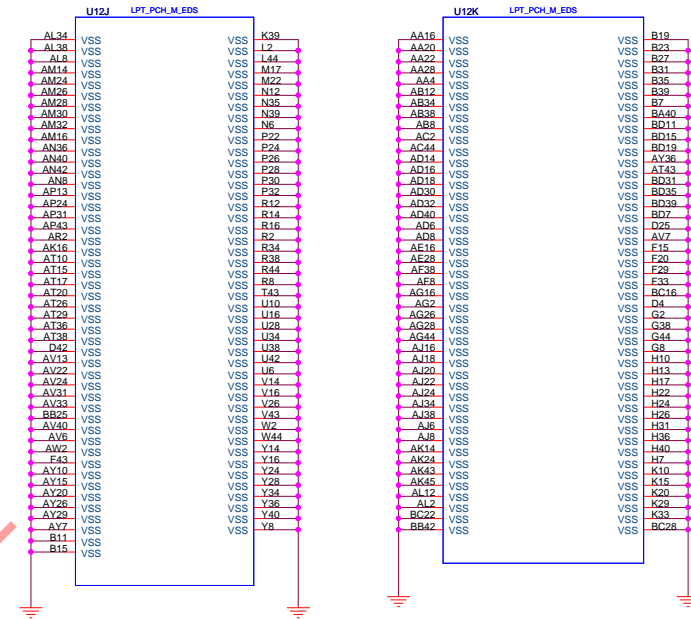
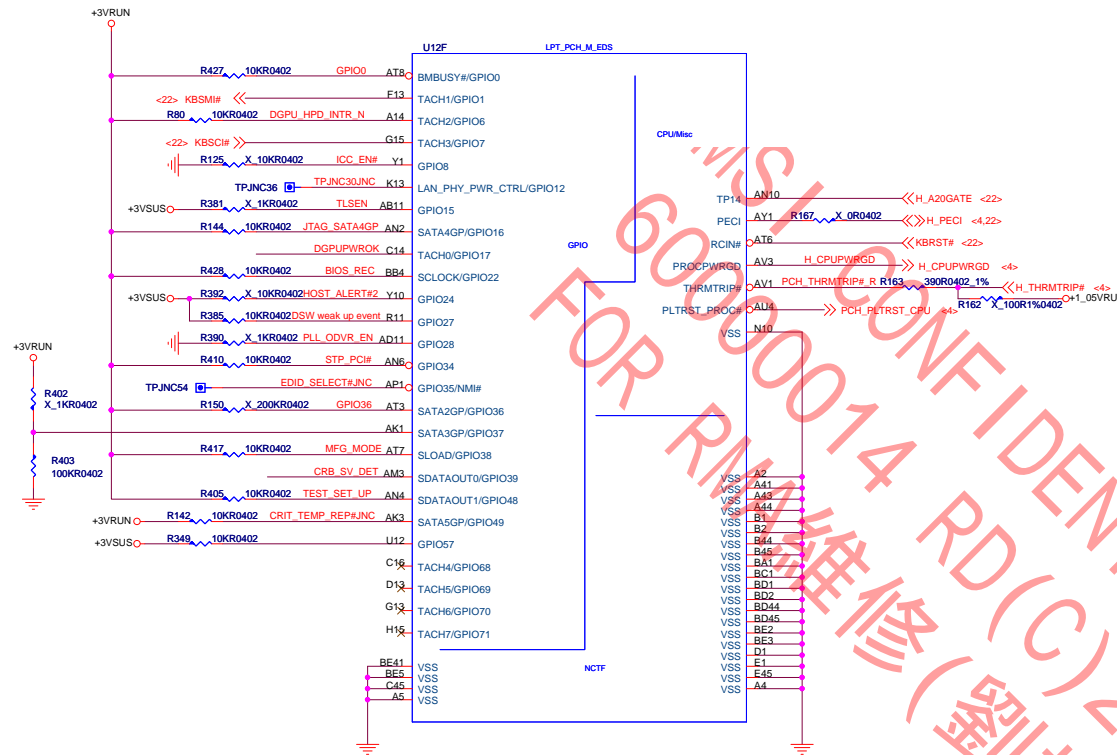


BBS_BIT0	BBS_BIT1	BOOT BIOS LOCATION
0	0	LPC
0	1	RESERVED(NAND)
1	0	N/A
1	1	SPI



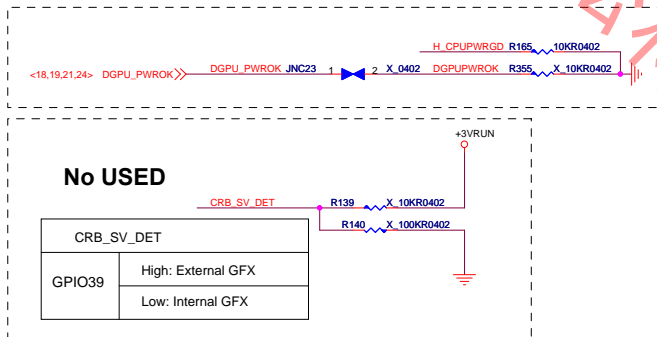
Lynx Point (GPIO,MISC)

Lynx Point (Gnd)



SATA3GP/GPIO37
This signal has a weak internal pull-down.
NOTE:
The internal pull-down is disabled after PLTRST# deasserts.
NOTE:
This signal should not be pulled high when strap is sampled.

This signal has a weak internal pull-down.
NOTE:
The internal pull-down is disabled after PLTRST# deasserts.
GPIO36 --CRB connector to 3V

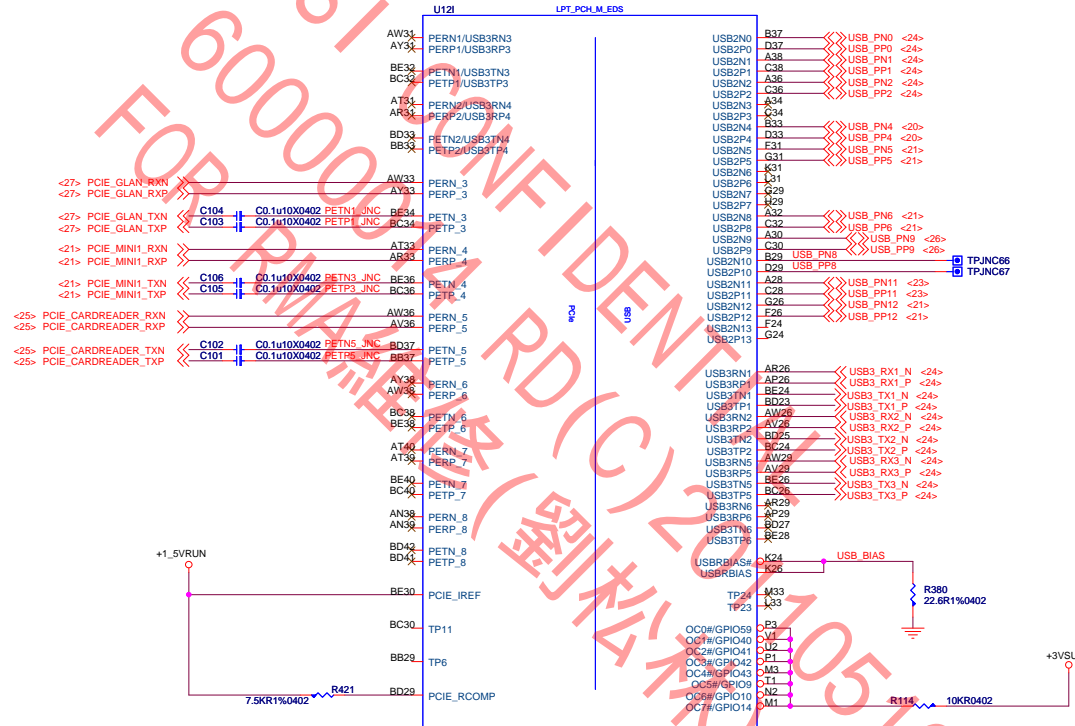


GPIO0 & 6 & 16 & 17 & 22 & 34 & 38 & 48 --If not used,require pull up 3VRUN
GPIO57 --If not used,require pull up 3VSUS
GPIO15--Not support AMT,Transport Layer Security Disable(High is support TLS,internal pull-down)
GPIO27 is deep S4 & S5 weak up event,internal pull high.& It's VCCFDIPLL internal VRM strapping pin
GPIO35 --Define to EDID Select (If not used,require pull down)

SATA2GP/GPIO36 (net name: FDI_OVRVLTG) & SATA3GP/GPIO37 (net name: SATA_ODD_PRSENT#)
Sampled at Rising edge of PWROK.
Weak internal pull-down. (weak internal pull-down is disabled after PLTRST# de-asserts)
NOTE: This signal should NOT be pulled high when strap is sampled

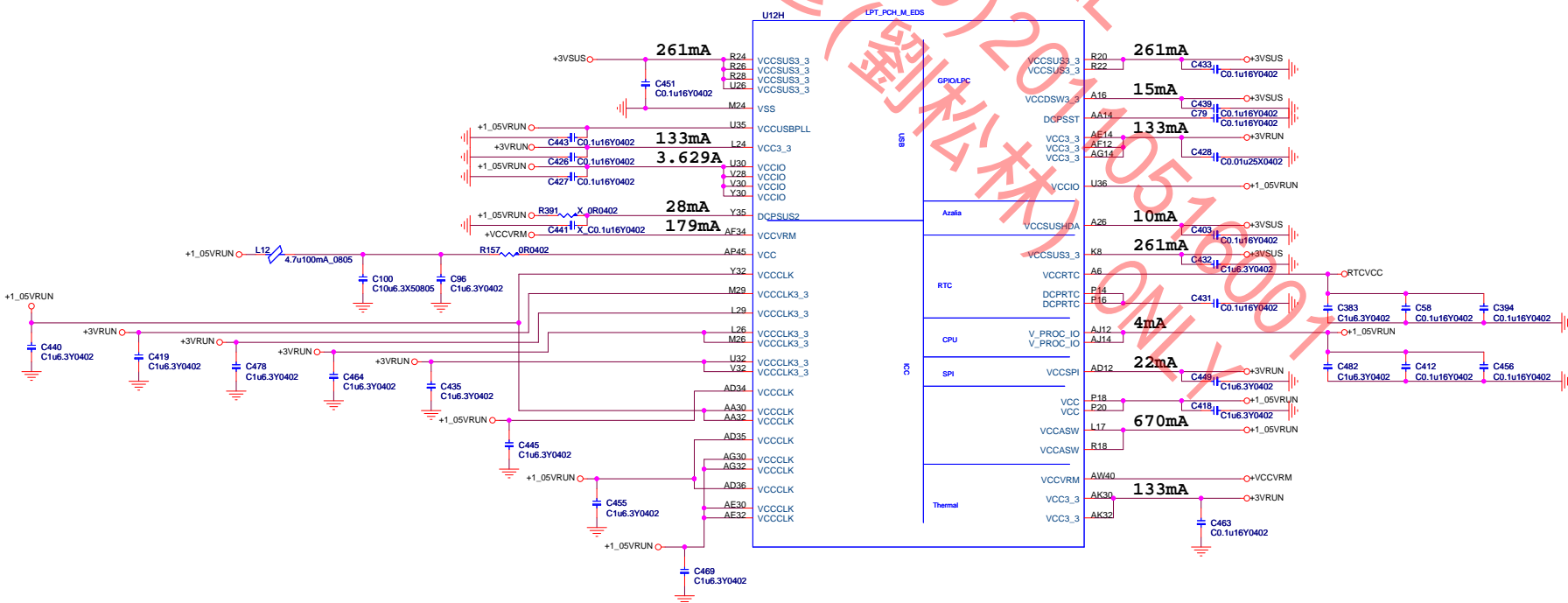
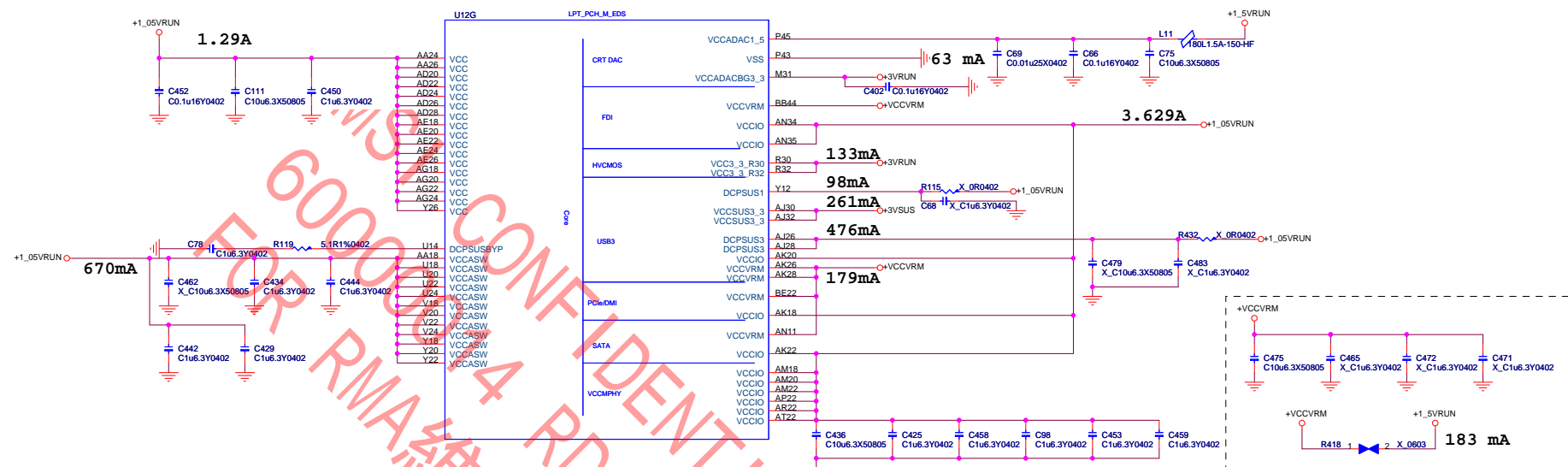
Lynx Point (PCIE,USB)

PCI-E	
Port	Device
3	Giga Lan
4	Mini PCIE-WLAN
5	Card Reader

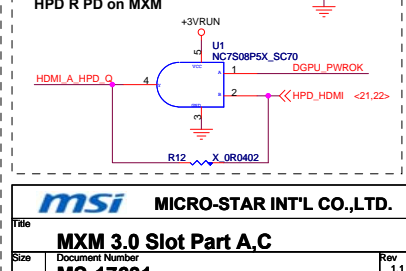
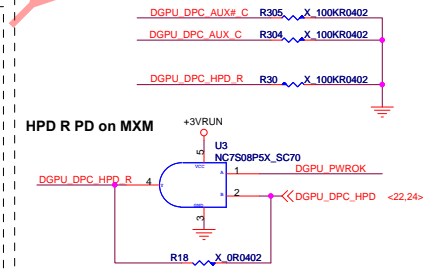
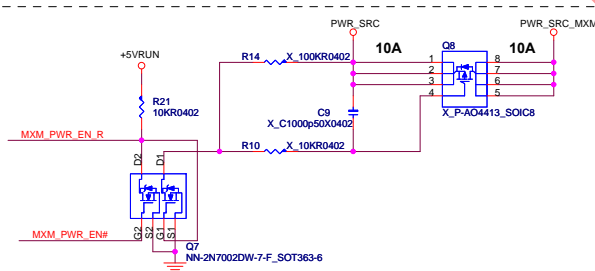
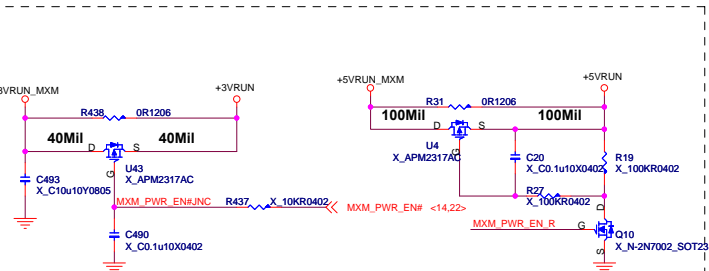
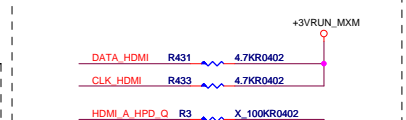
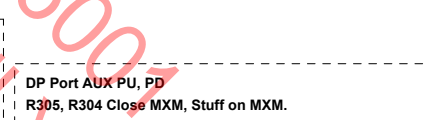
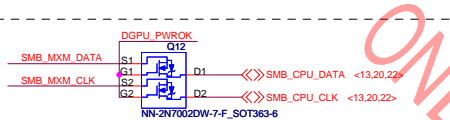
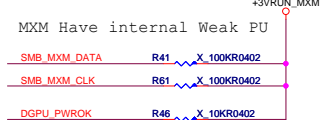


USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	
1	2	USB 3.0 Port 2	Debug Port
2	5	USB 3.0 Port 3	
3			NC
4		WebCam (LVDS)	
5		USB 2.0 Port 5 (1763)	
6			NC
7			NC
8		USB 2.0 Port 5 (1763)	
9		USB 2.0 Port 5 (16F4)	Debug Port
10		TestPad	
11		EPF LED (8051)	
12		Mini PCIE-BT	
13			NC
	3		NC
	4		NC
	6		NC

Lynx Point (Power)



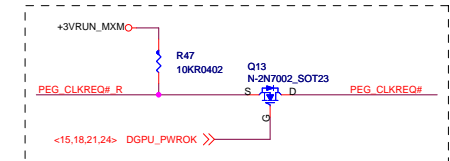
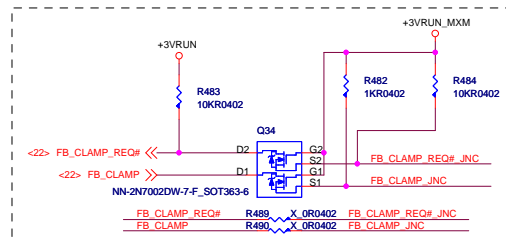
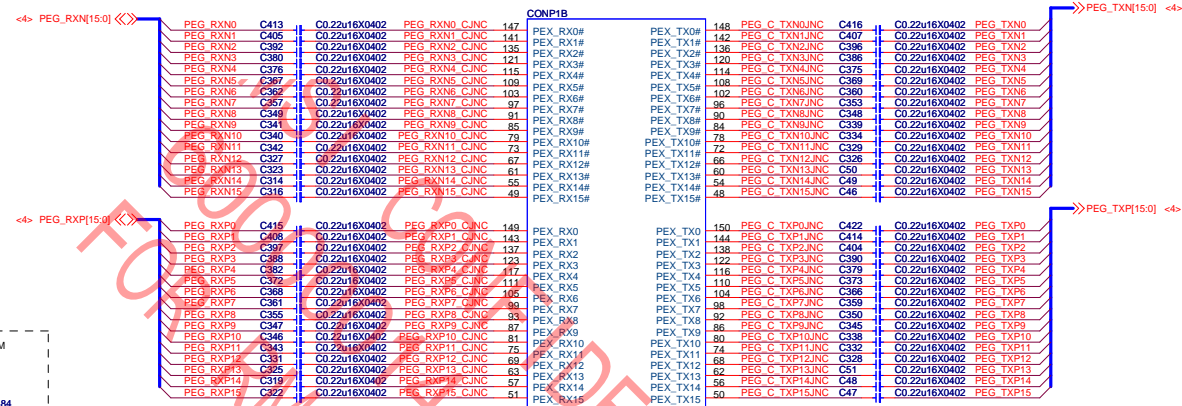
MXM 3.0 (x16 PEG Gen 3)



MXM 3.0 (x16 PEG Gen 3)

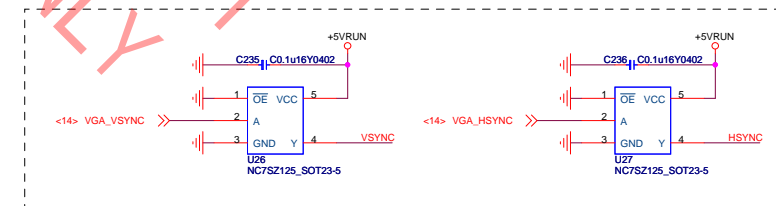
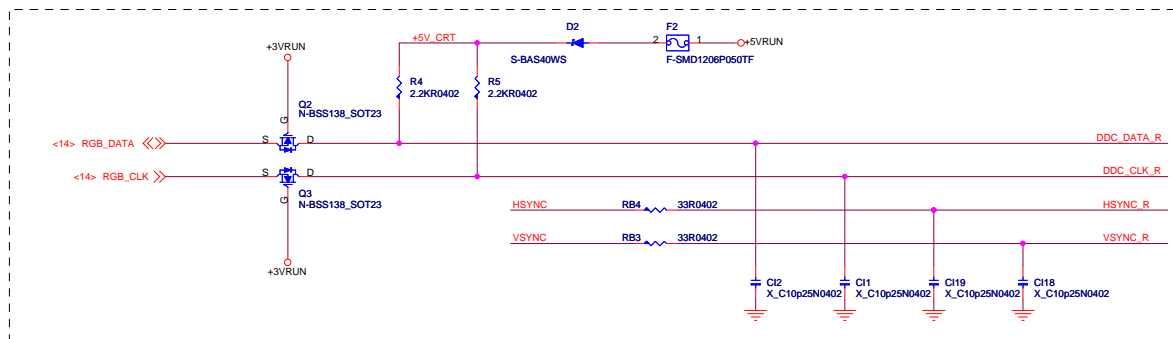
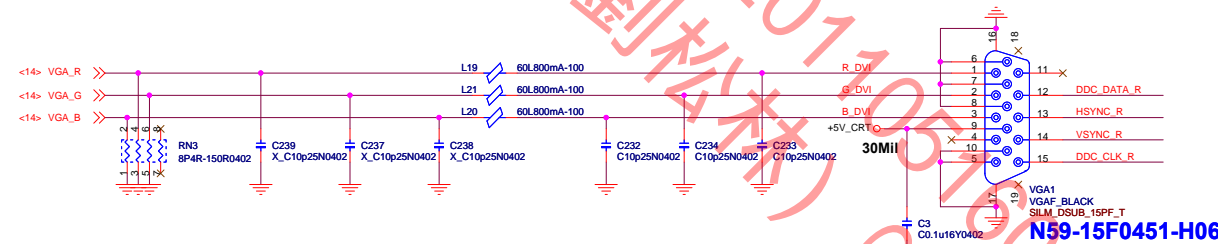
n'VIDIA Comments: NV11 can't support PCIE GEN3,so used 0.1uf CAP

The change in AC capacitor value from 0.1uf to 0.22uf is to enable compatibility with future platforms having PCIE GEN3(8GT/s)

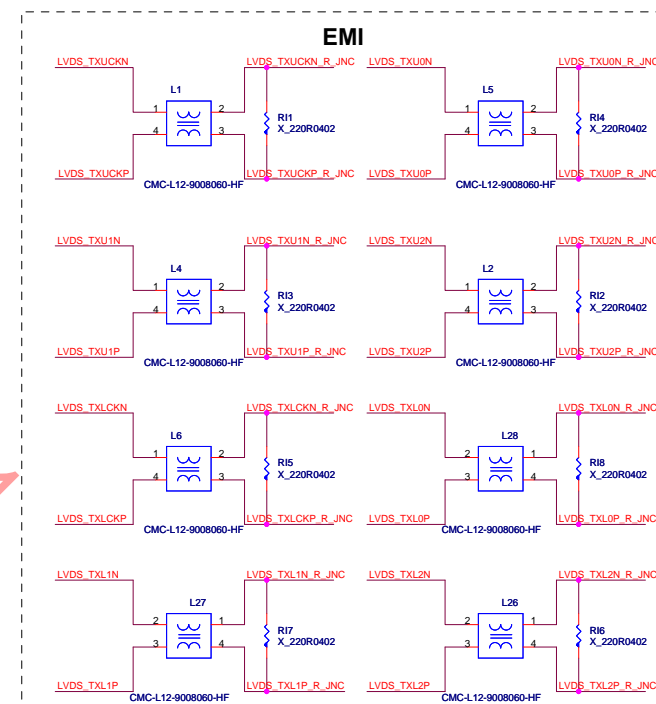
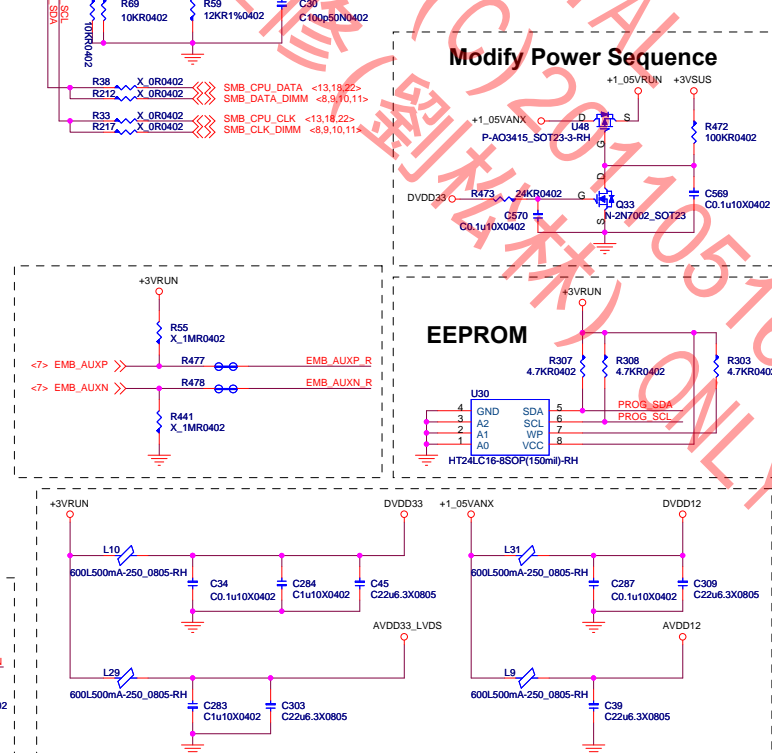
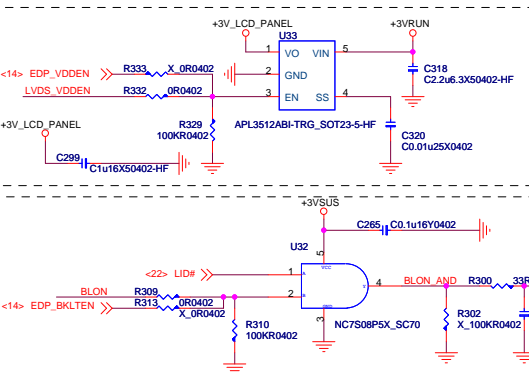
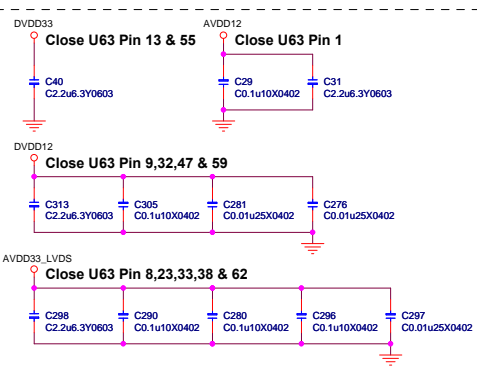
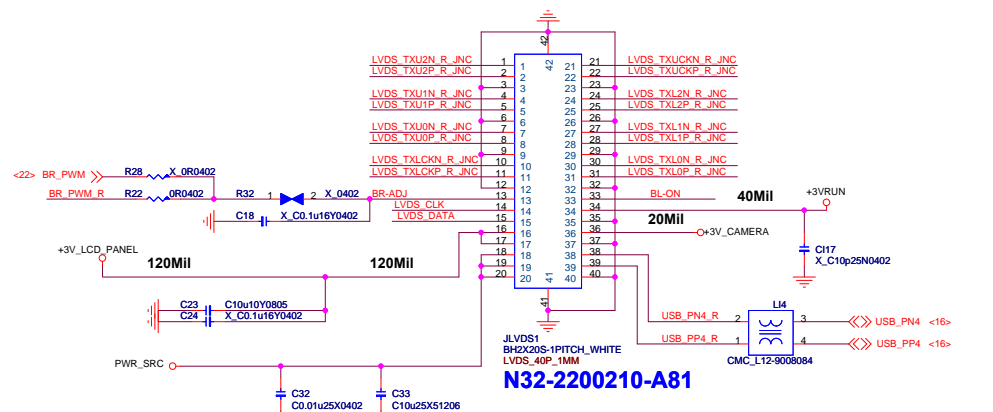
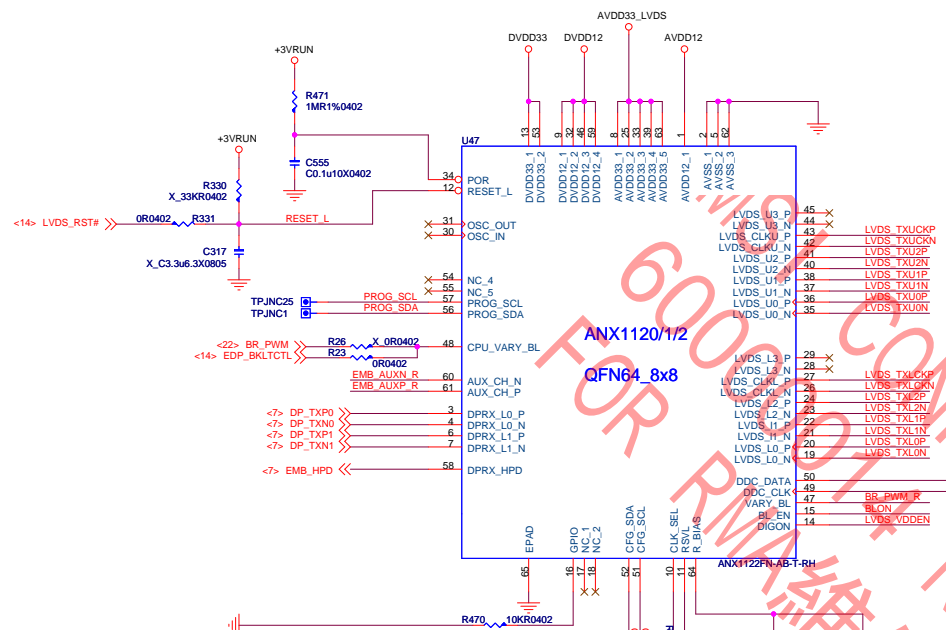


SLOT-MXM314P-0.5PITC
N11-3140030-A81

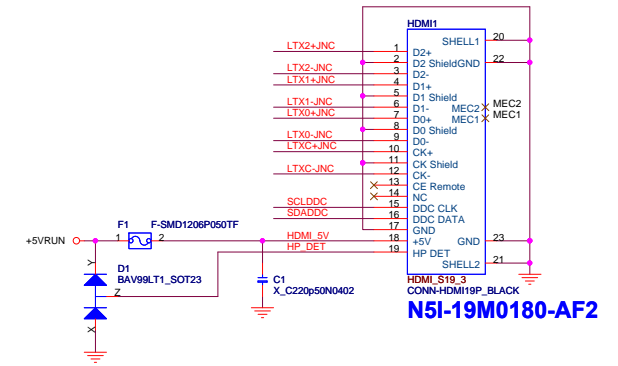
CRT



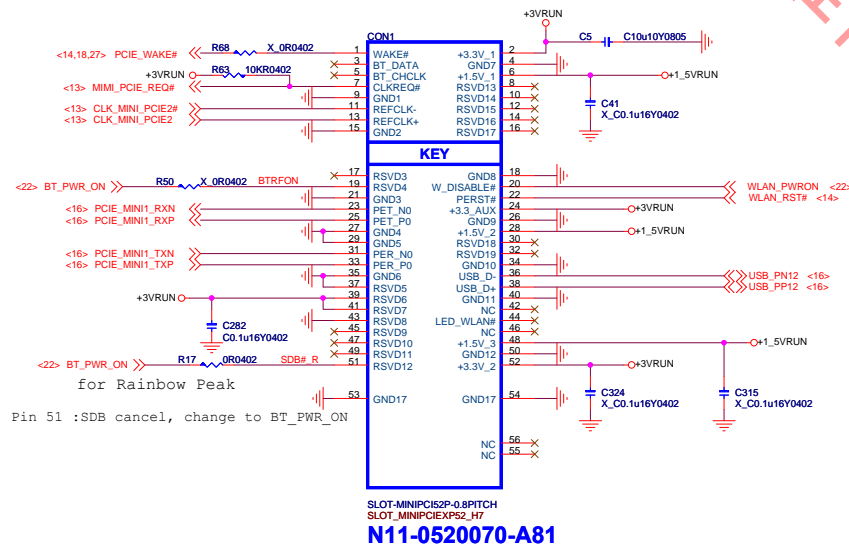
eDP to LVDS



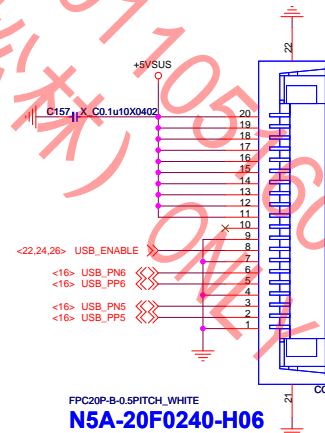
WLAN/BT



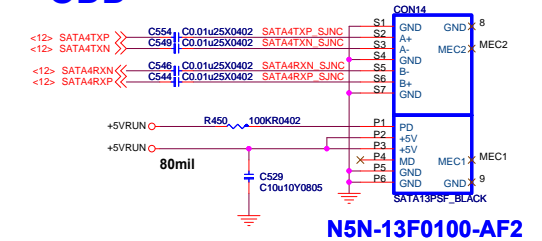
WLAN/BT



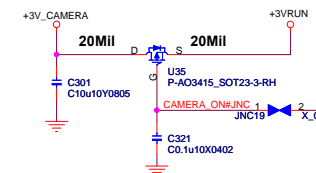
**MS-1763 Co-Lay
USB Port *2**



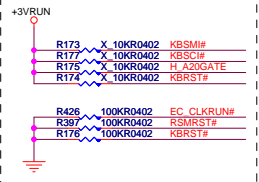
ODD



WebCAM



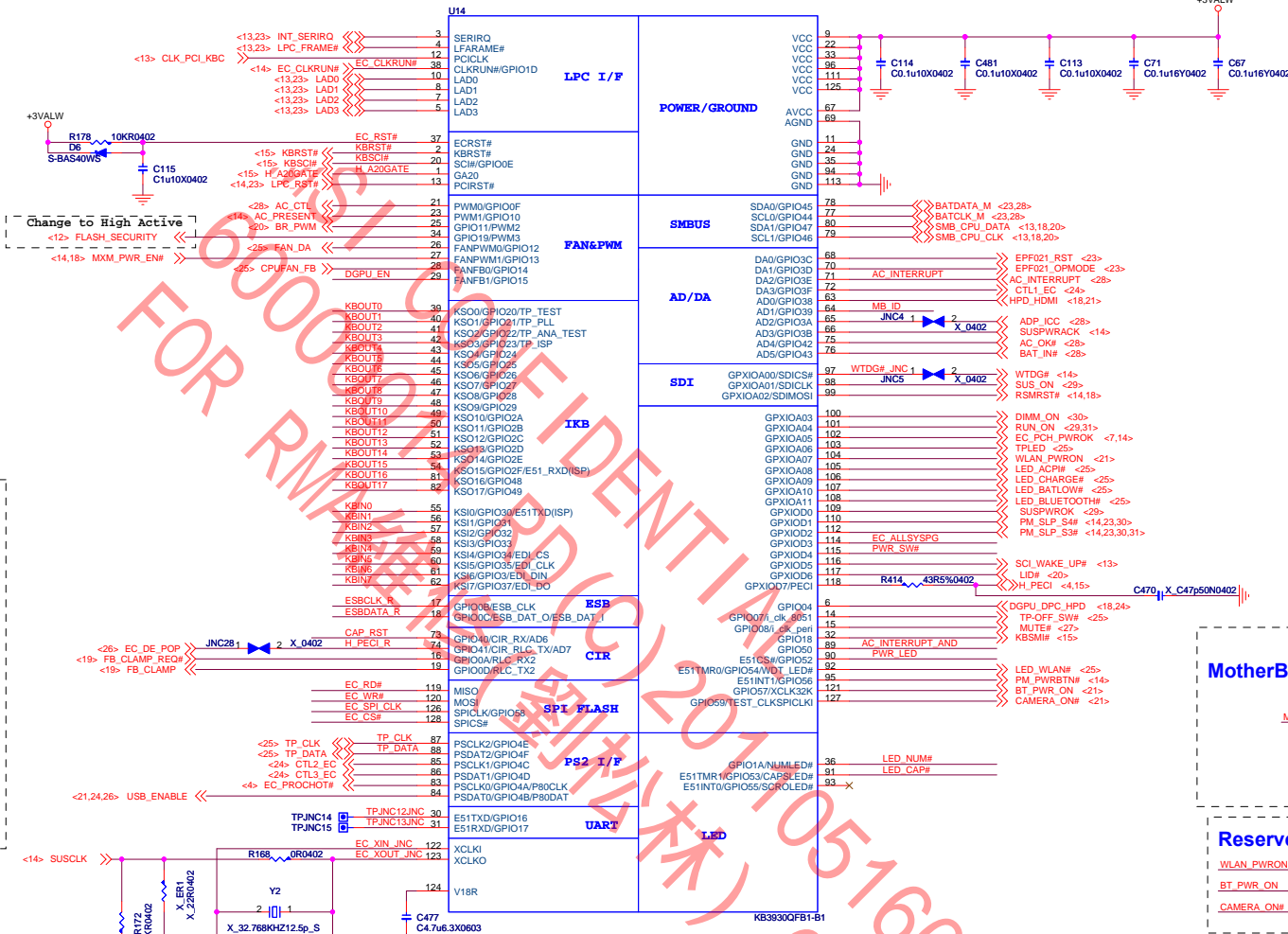
PU/PD



N71-0101630-D02

[illegible][illegible]

Pin 14 connection diagram for N32-1140160-A81. The diagram shows a 14-pin connector with pins 1 through 14. Pin 1 is LPC_FRAME#, pin 2 is LAD3, pin 3 is LAD2, pin 4 is LAD1, pin 5 is LAD0, pin 6 is L_LDRQ0#, pin 7 is INT_SERIRQ, pin 8 is LPC_RST#, pin 9 is empty, pin 10 is +5VRUN, pin 11 is +3VRUN, pin 12 is FWH_ID0, pin 13 is empty, and pin 14 is empty. The connector is connected to a board with pins 1 through 14. Pin 14 is connected to a 1kR0402 resistor and a 5V supply. The board is labeled N32-1140160-A81.



Pinout diagram for the N5A-26F0340-A81 connector. The diagram shows a 26-pin connector with pins numbered 1 to 26. The pins are labeled as follows:

Pin Number	Signal Name
26	KBOUT17
25	KBOUT16
24	KBIN0
23	KBIN1
22	KBIN2
21	KBIN3
20	KBIN5
18	KBIN6
17	KBIN7
16	KBOUT15
15	KBOUT14
14	KBOUT13
13	KBOUT12
12	KBOUT11
11	KBOUT10
10	KBOUT9
9	KBOUT5
8	KBOUT7
7	KBOUT6
6	KBOUT5
5	KBOUT4
4	KBOUT3
3	KBOUT2
2	KBOUT1
1	KBOUT0

The connector is shown in a side view with a blue outline. A ground symbol is shown at the bottom right, and a CN1 label is at the top right.

The figure displays two schematic diagrams of photonic structures. The top diagram, labeled '8P4C-100pS/50nM40Z', shows four input/output pairs: KBOUT17/EC11, KBOUT16/EC12, KBOUT7/EC15, and KBOUT6/EC14. The bottom diagram, labeled '8P4C-100pS/50nM40Z+', shows four input/output pairs: KBOUT13/EC16, KBOUT12/EC17, KBOUT9/EC14, and KBOUT8/EC13. Each diagram includes a table of port numbers and a corresponding circuit schematic.

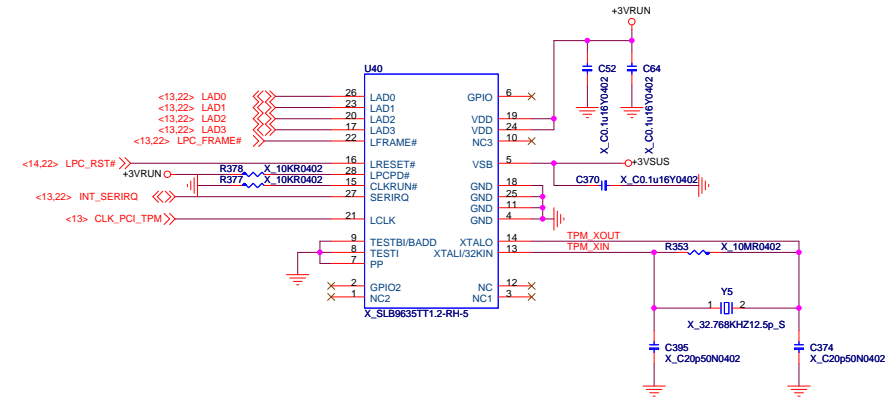
Port	Port	Port	Port
KBOUT17	EC11	C100pS/50nM40Z	KBOUT16
KBOUT16	EC12	C100pS/50nM40Z	KBOUT7
KBOUT7	EC15		KBOUT6
KBOUT6	EC14		KBOUT4

8P4C-100pS/50nM40Z

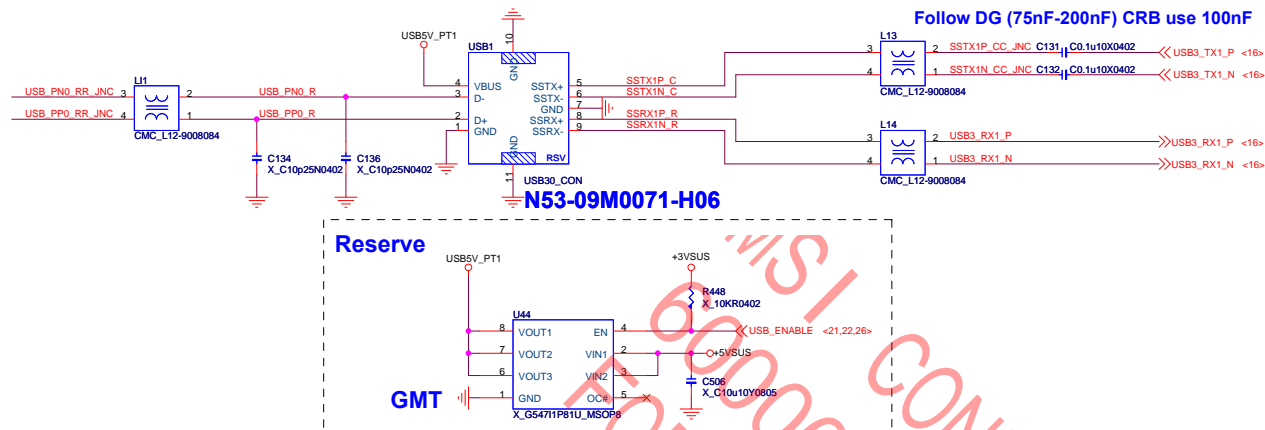
Port	Port	Port	Port
KBOUT13	EC16	C100pS/50nM40Z+	KBOUT12
KBOUT12	EC17		KBOUT9
KBOUT9	EC14		KBOUT8
KBOUT8	EC13		

8P4C-100pS/50nM40Z+

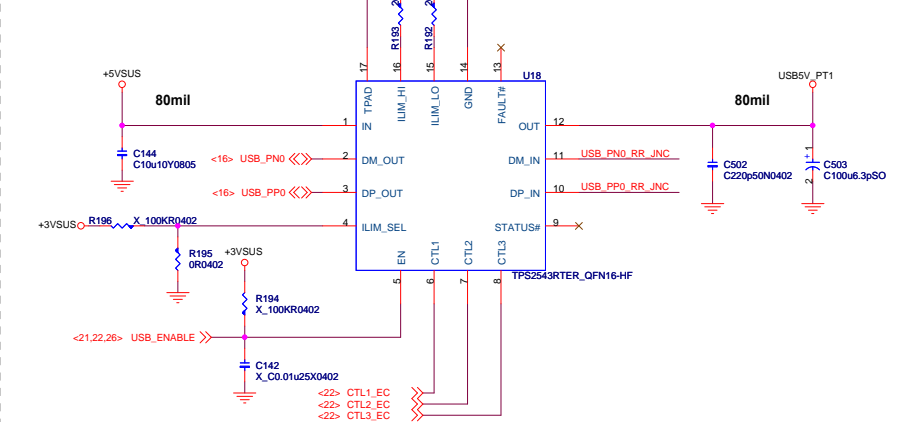
TPM



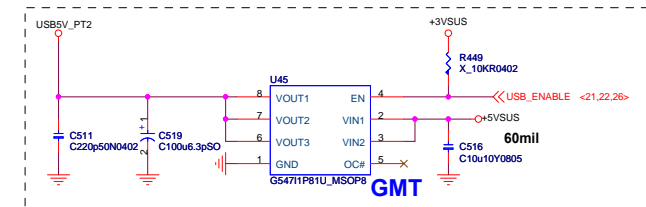
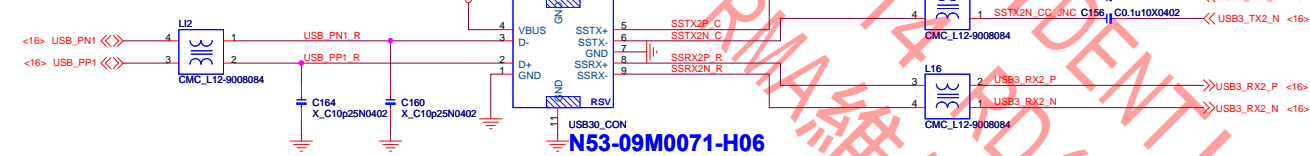
USB3.0 Port 1



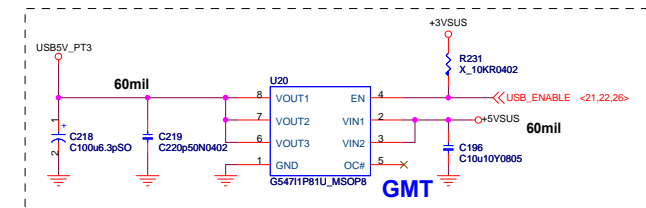
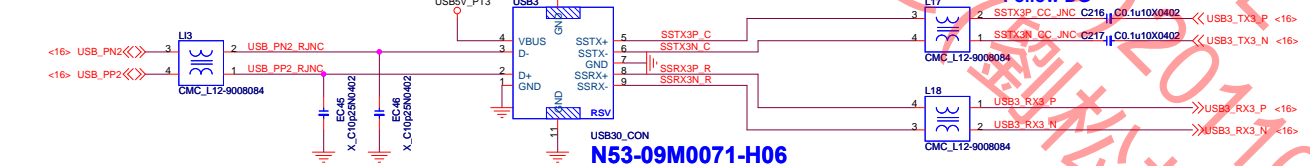
iPad Charger(Port1)



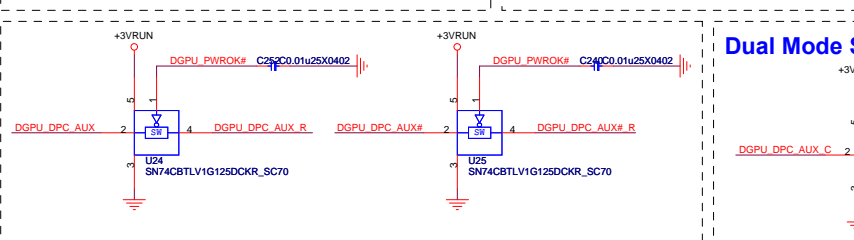
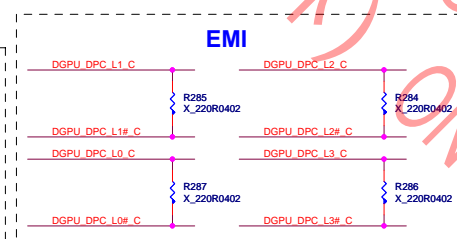
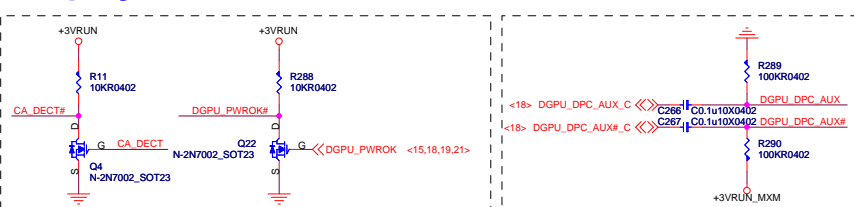
USB3.0 Port 2



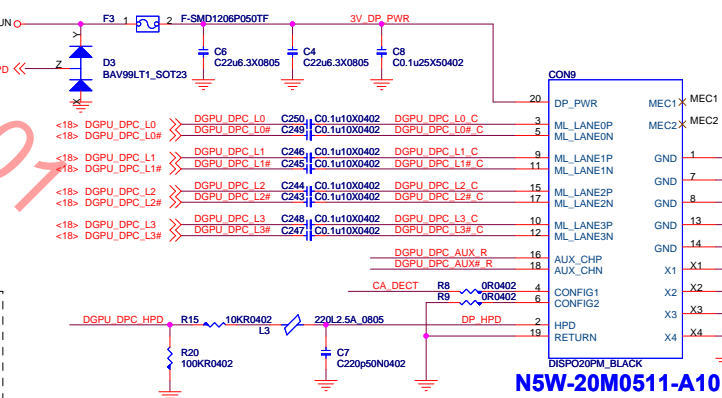
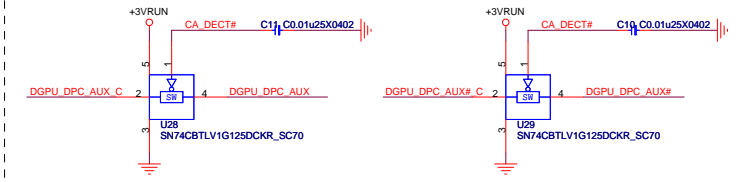
USB3.0 Port 3



Display Port



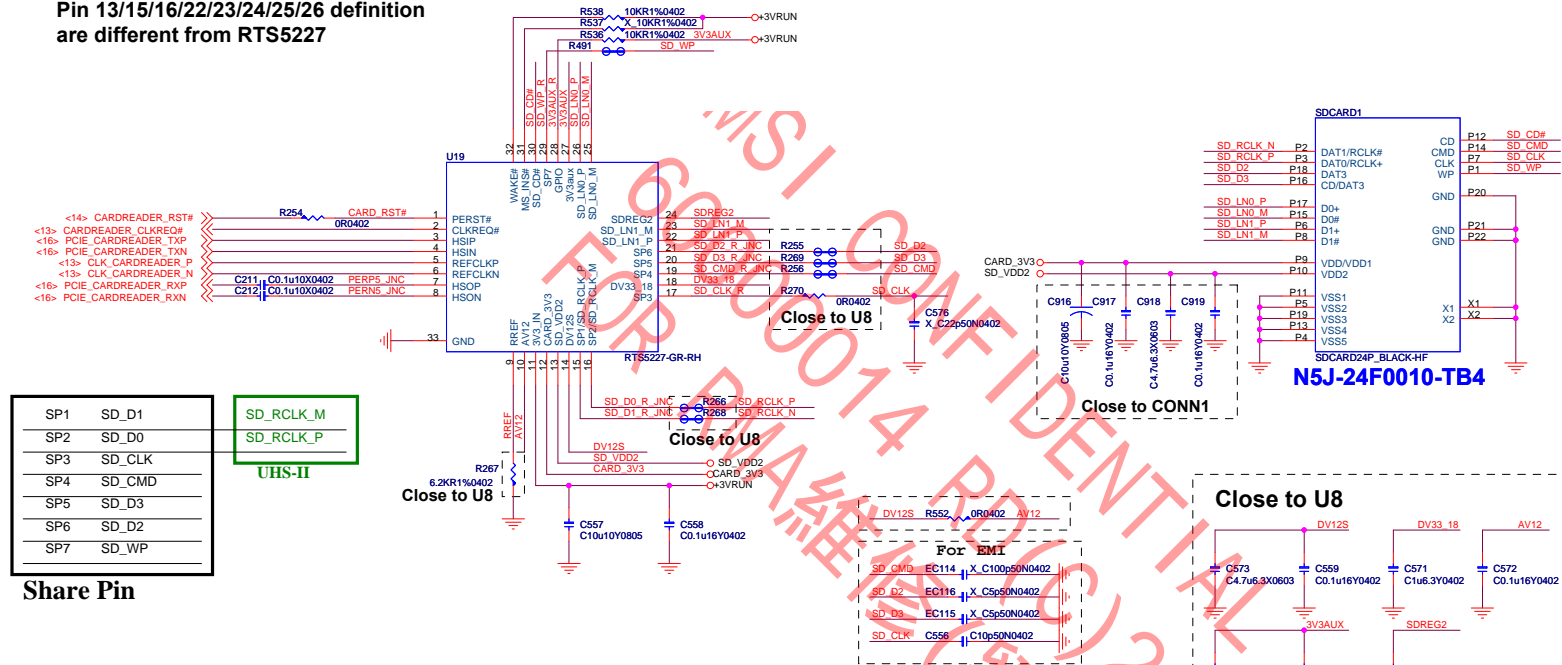
Dual Mode Switch



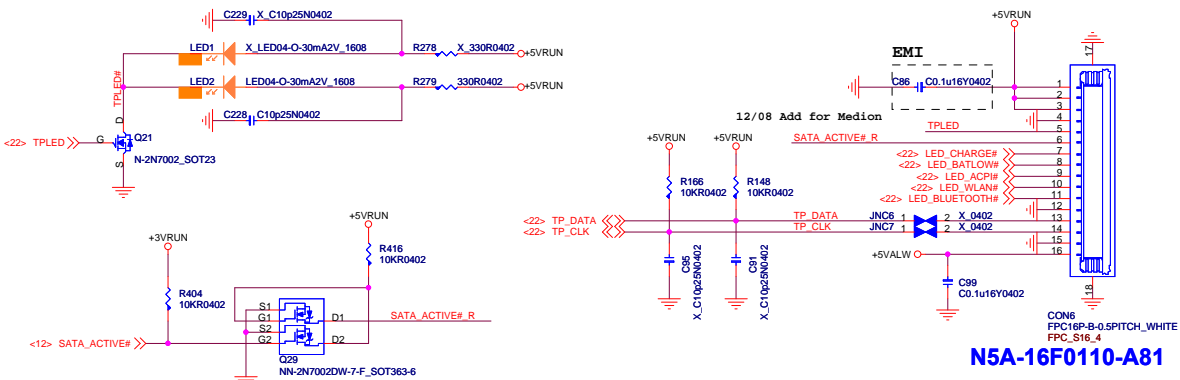
Card Reader(RTS5227)

RTS5249 Colay RTS5227

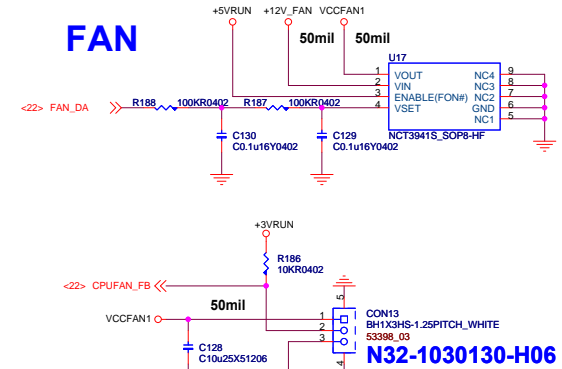
Pin 13/15/16/22/23/24/25/26 definition are different from RTS5227



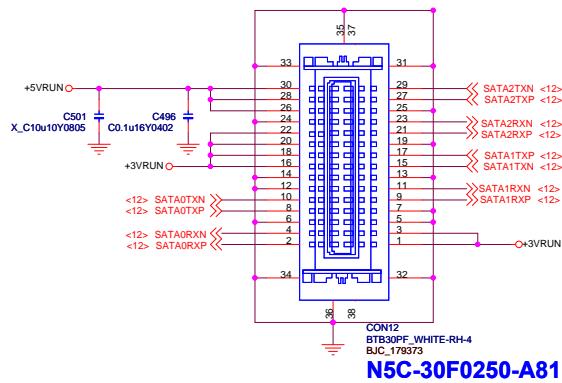
Touch Pad L/R-LED (Unmount)



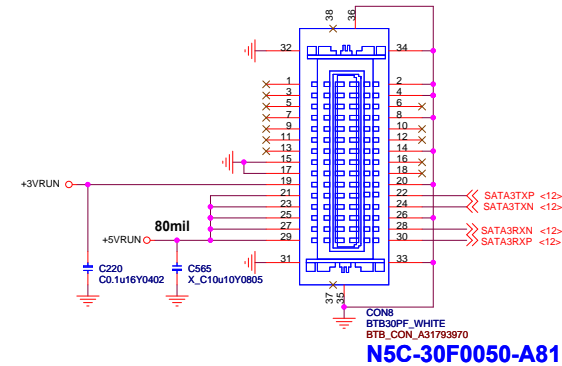
FAN



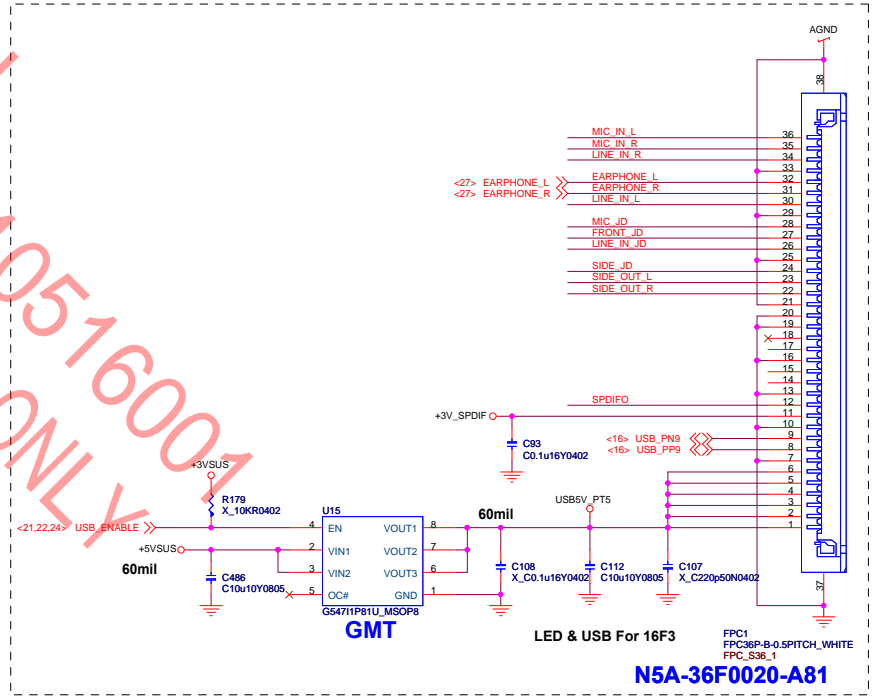
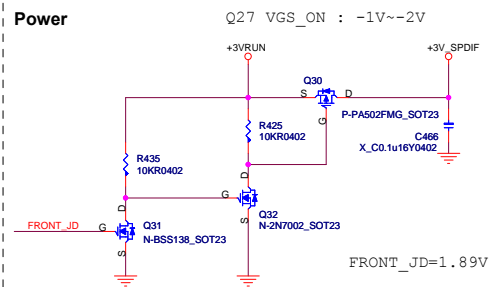
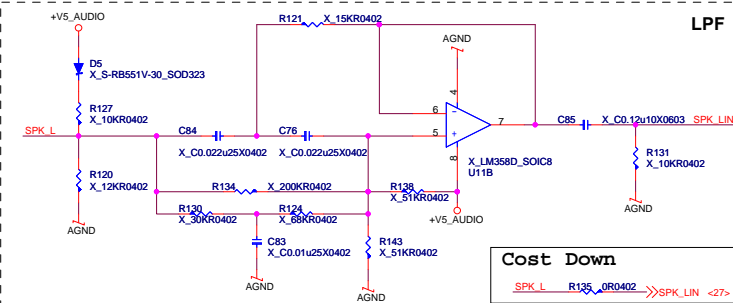
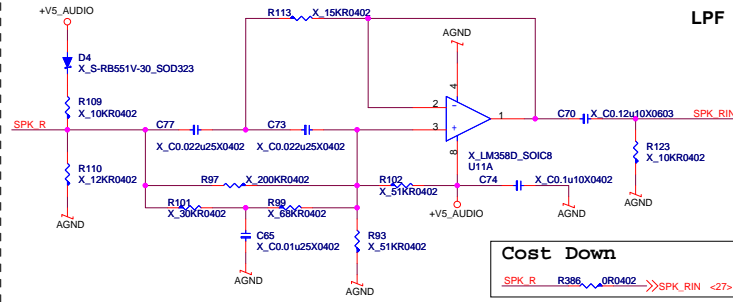
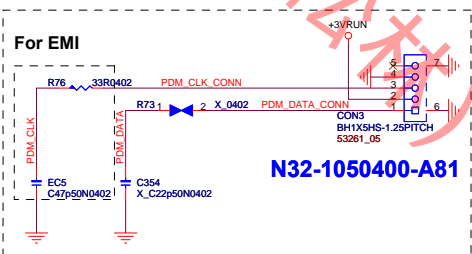
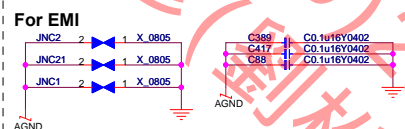
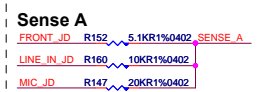
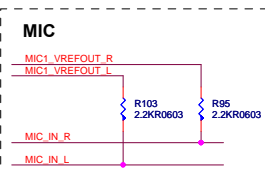
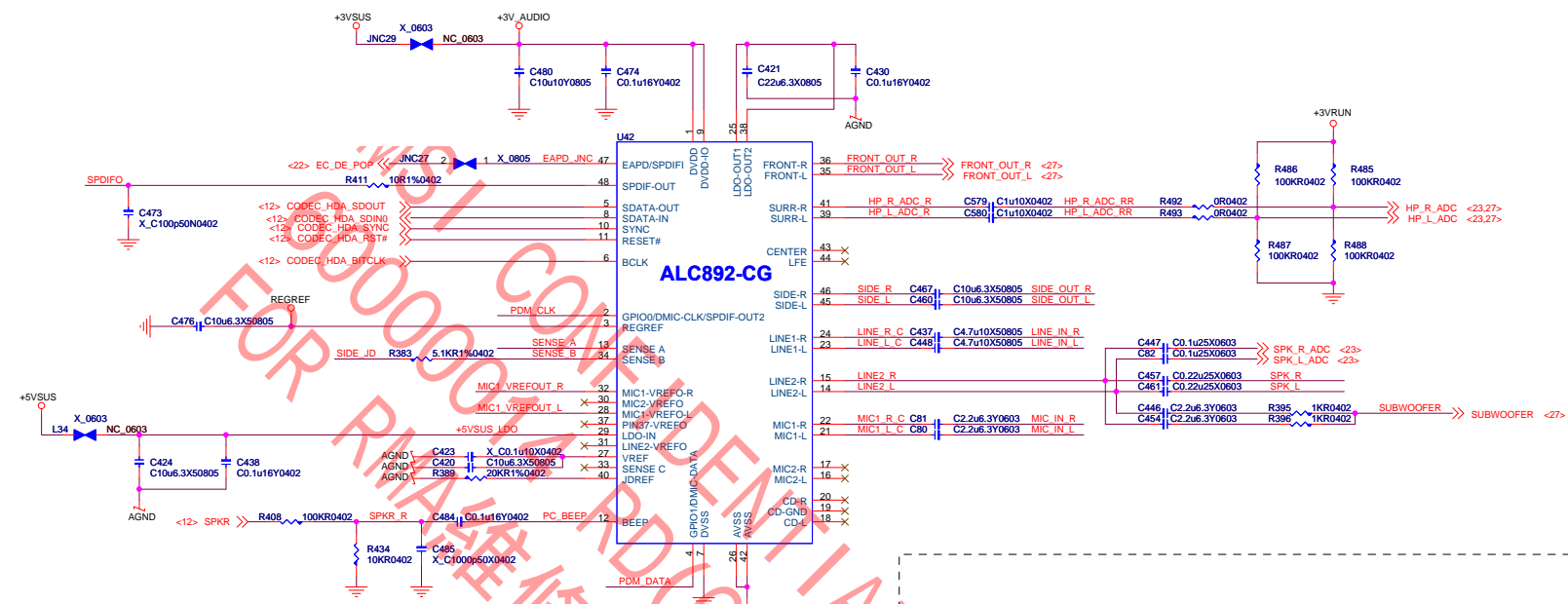
SATA HDD2 From Port 0,1,2



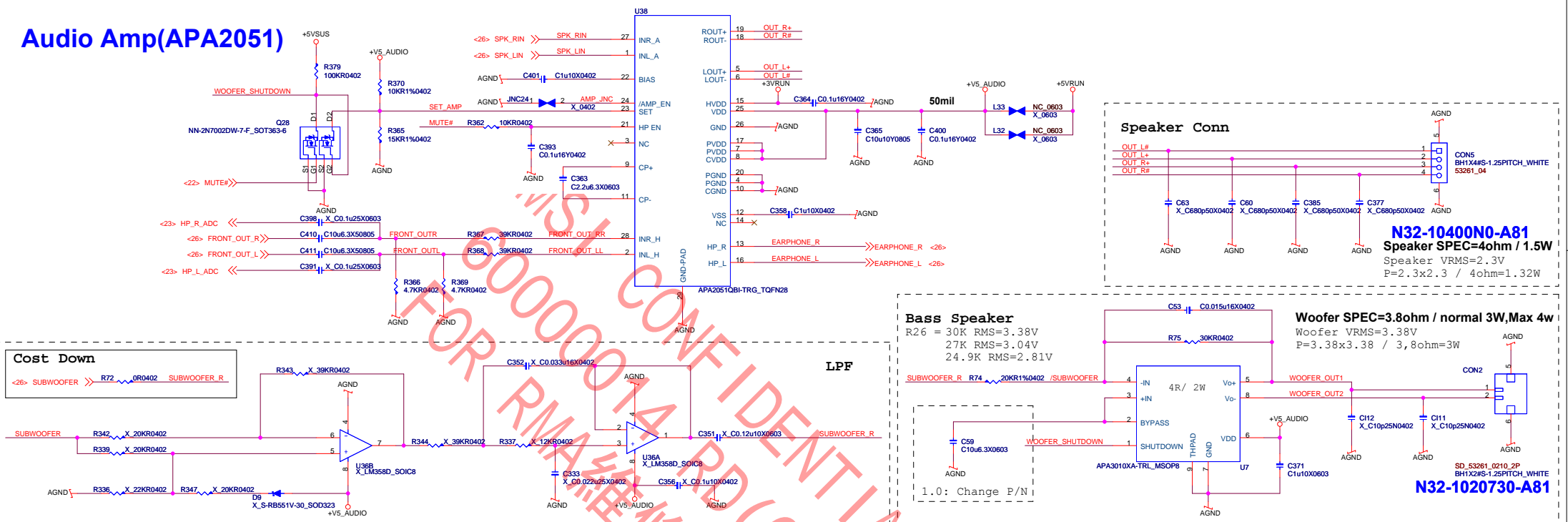
SATA HDD1 From Port 3



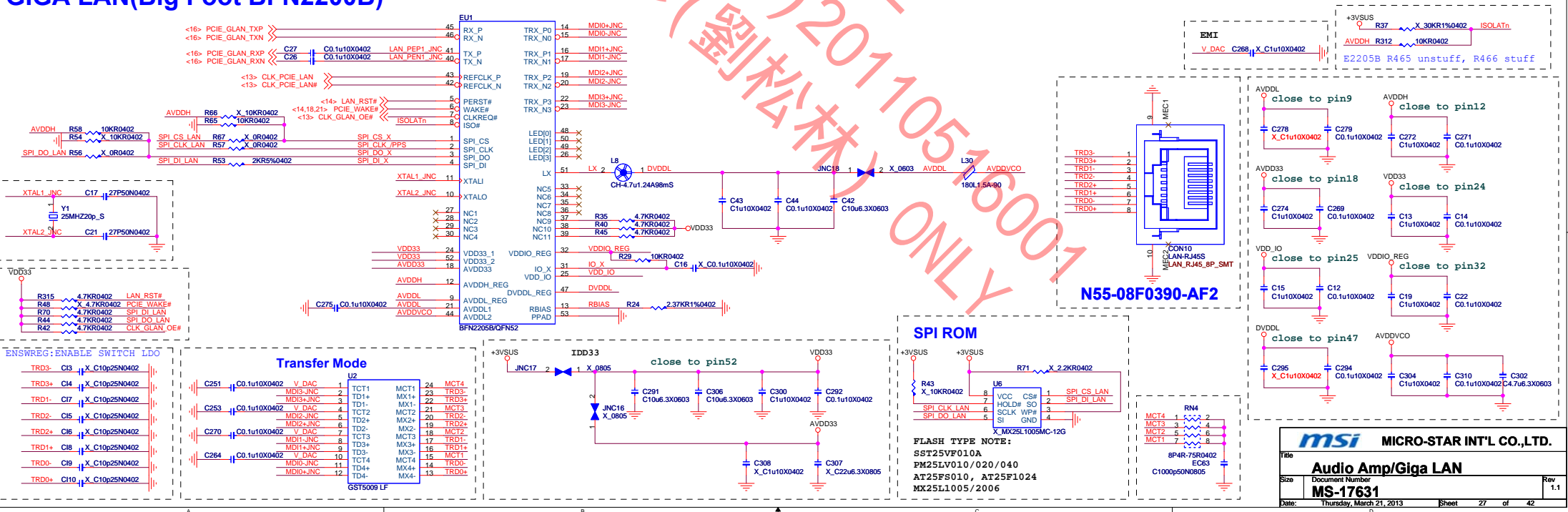
Azailia Codec(ALC892)



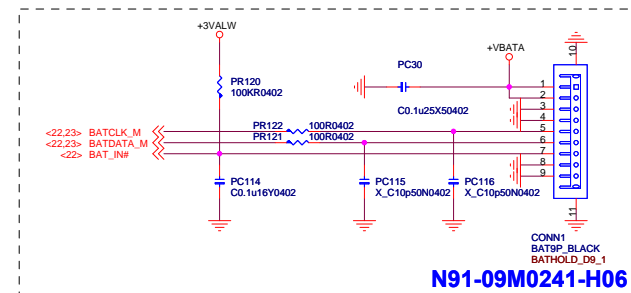
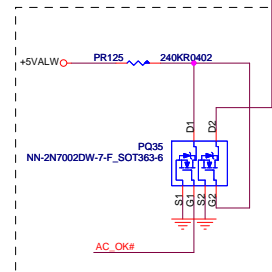
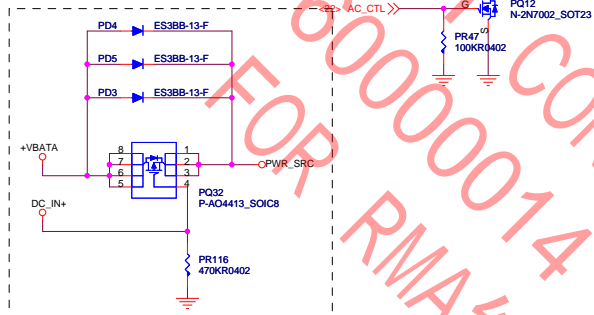
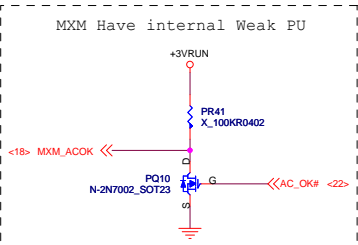
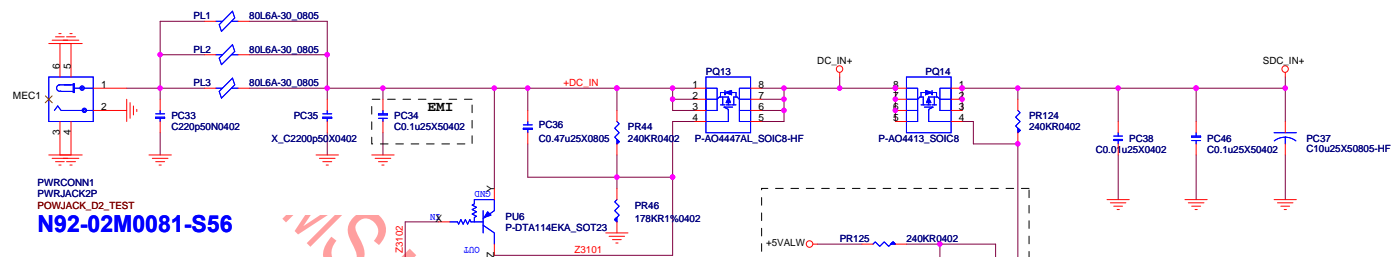
Audio Amp(APA2051)



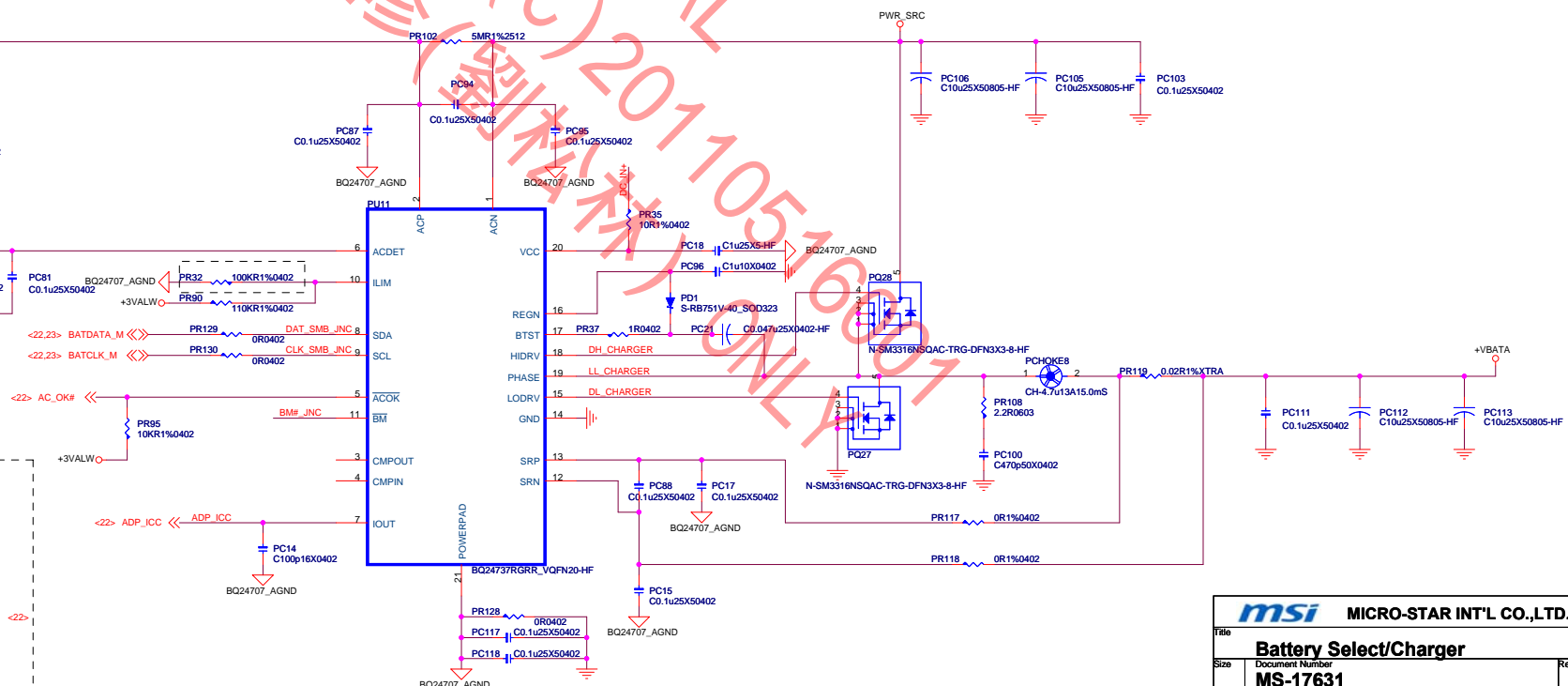
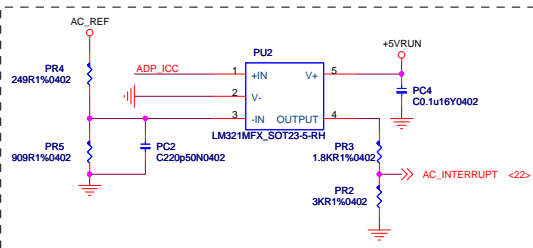
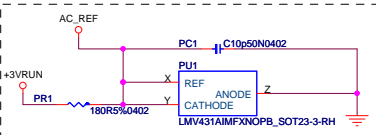
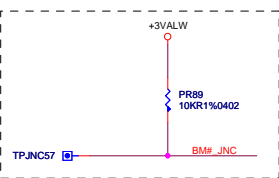
GIGA LAN(Big Foot BFN2200B)



Battery Select



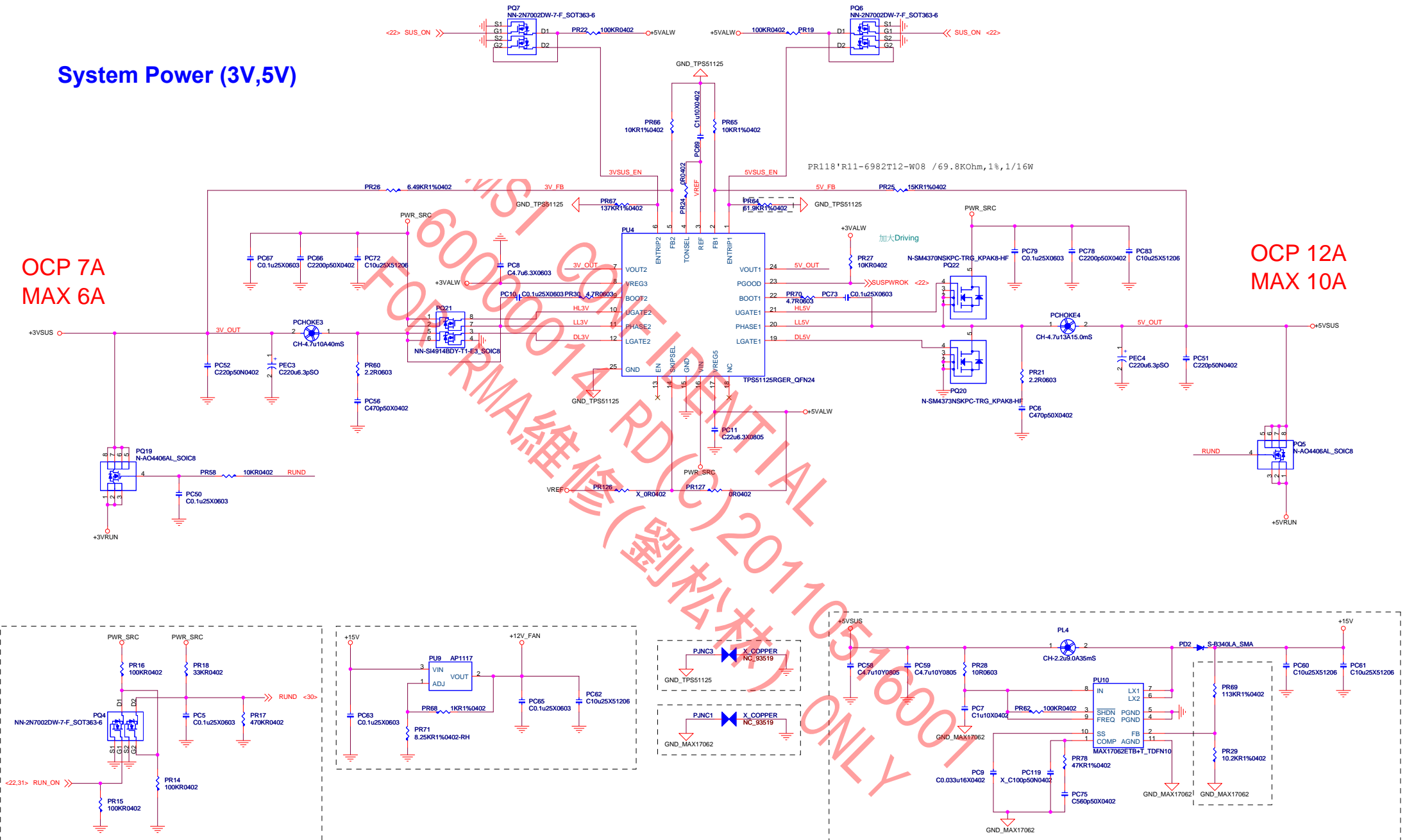
Battery Charger



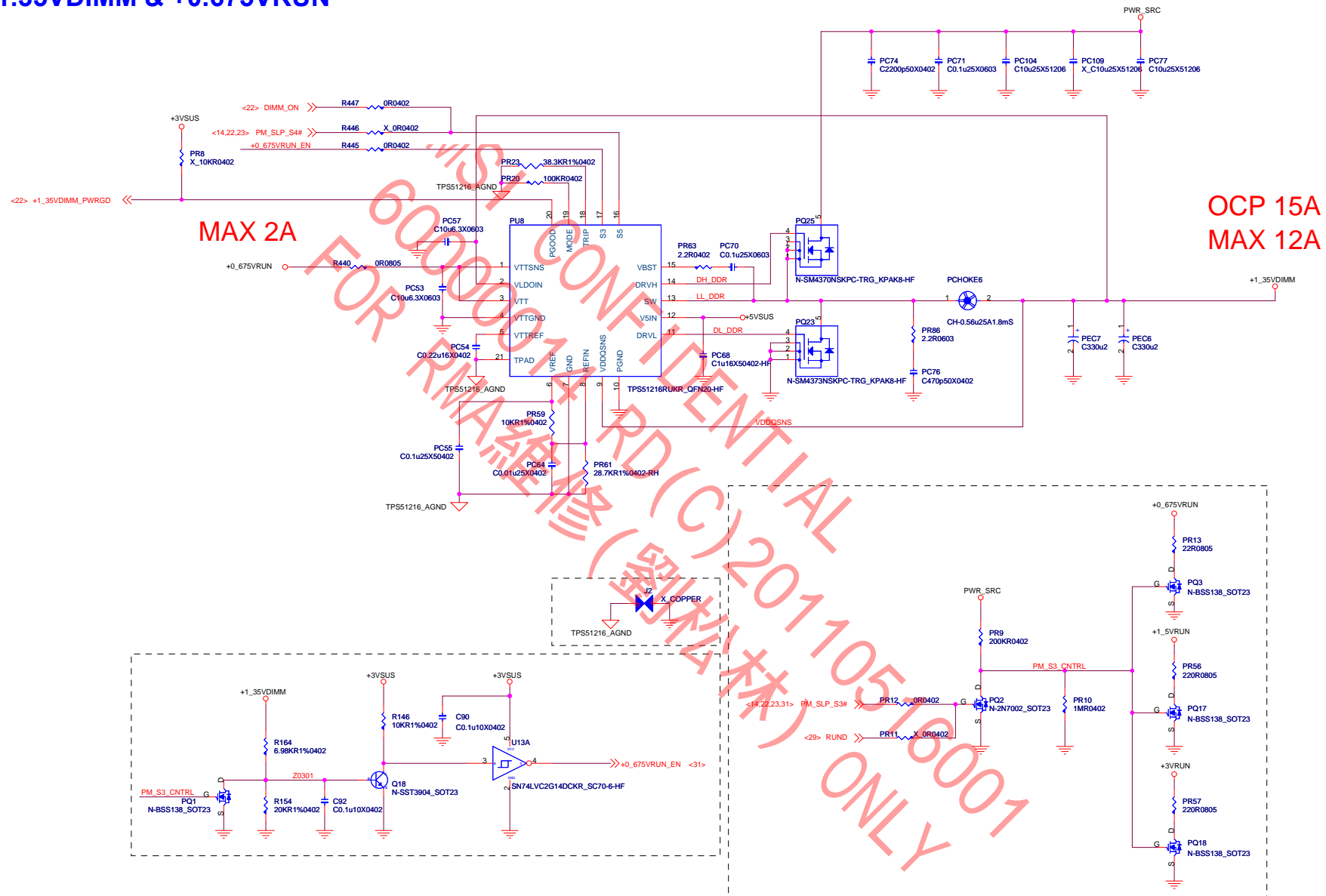
System Power (3V,5V)

OCP 7A
MAX 6A

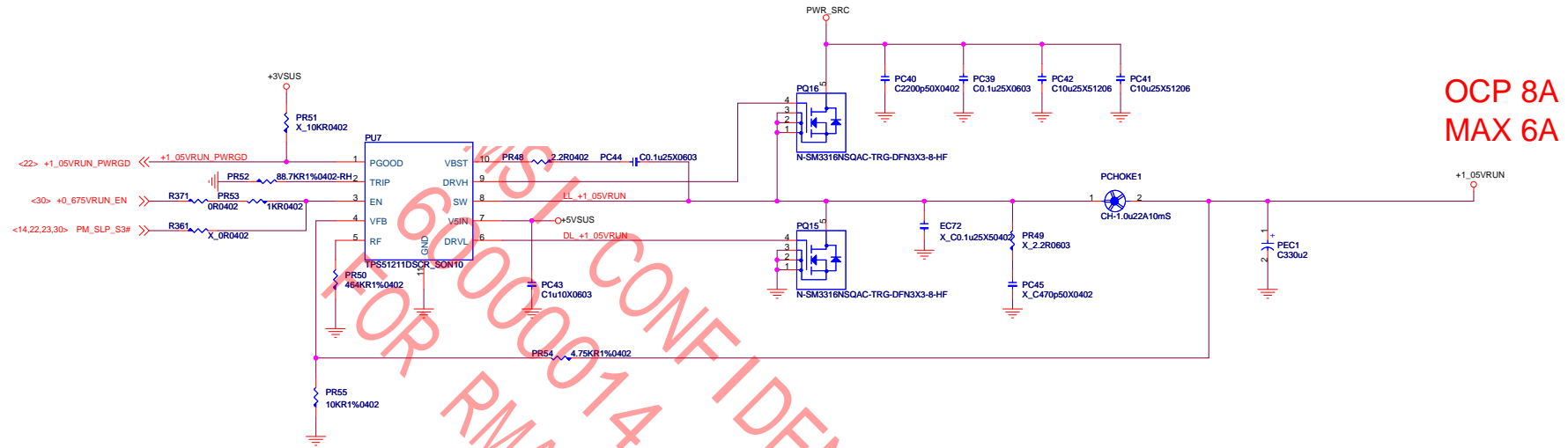
OCP 12A
MAX 10A



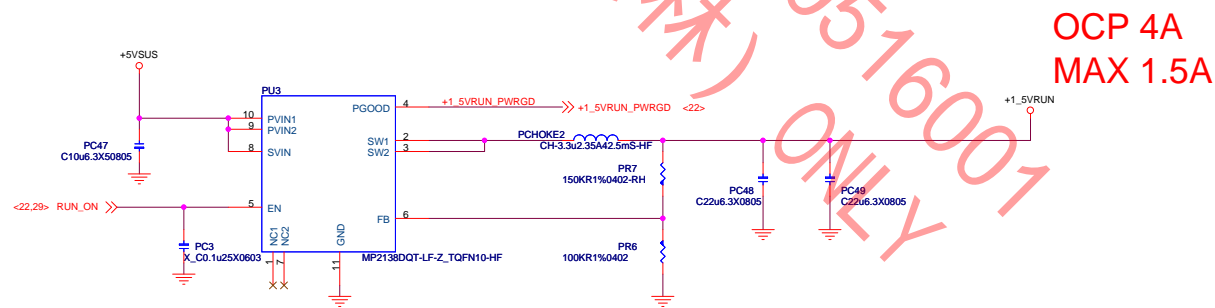
+1.35VDIMM & +0.675VRUN



+1.05VRUN



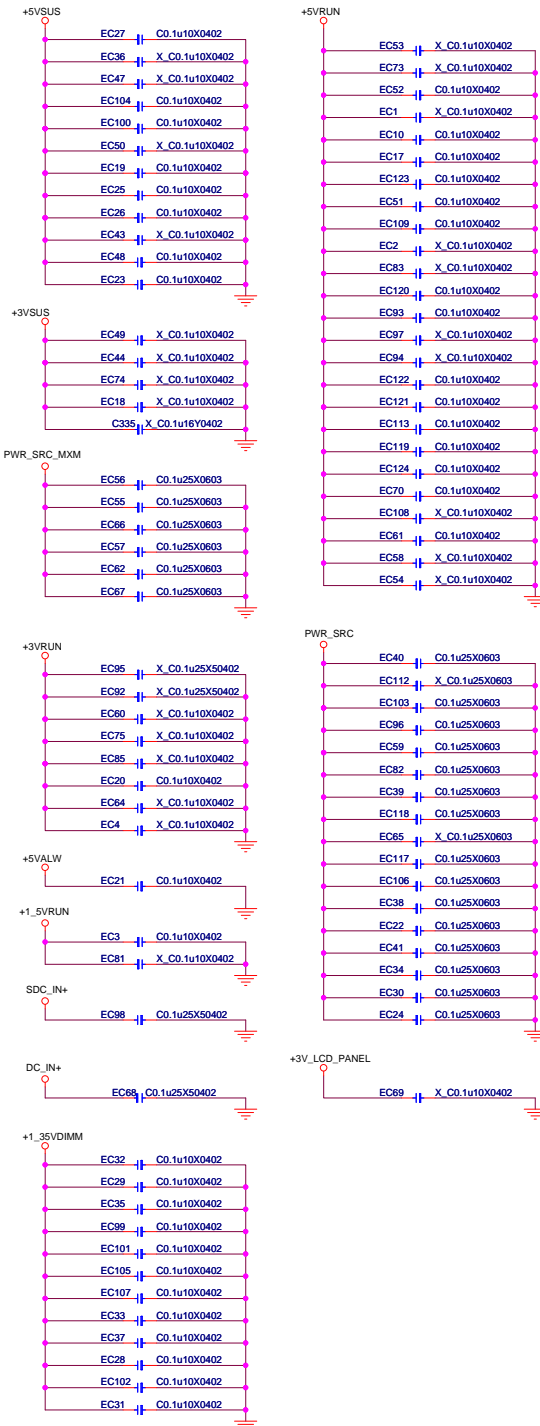
+1.5VRUN



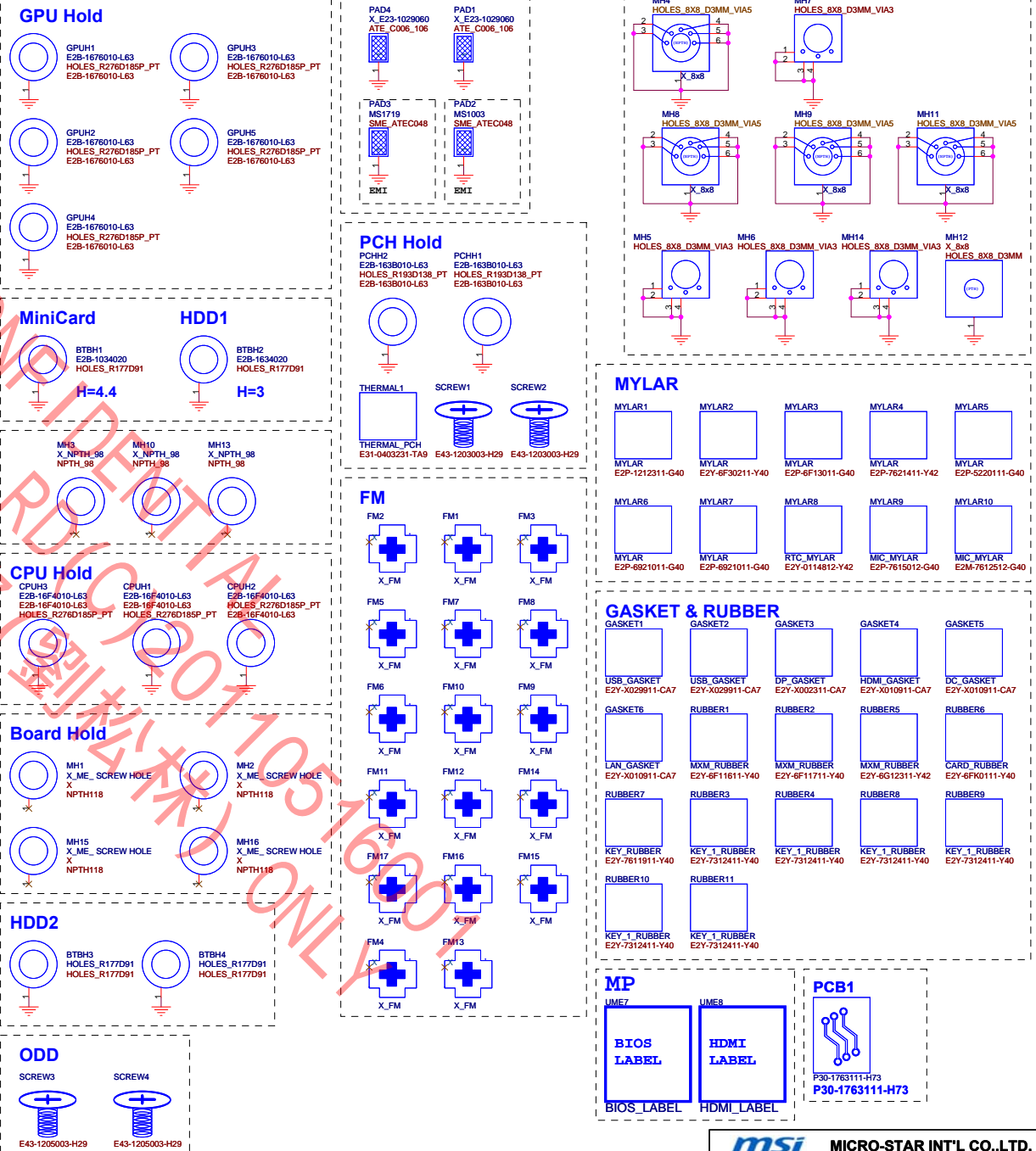
CPU Core Power(ISL95812HRZ)



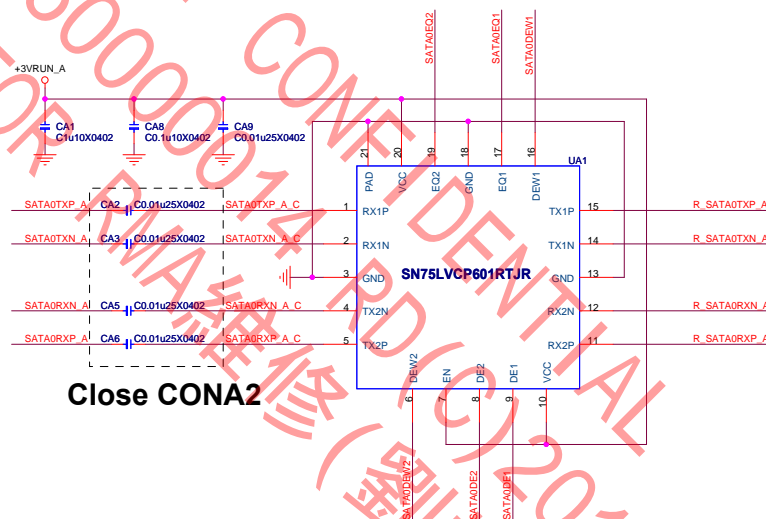
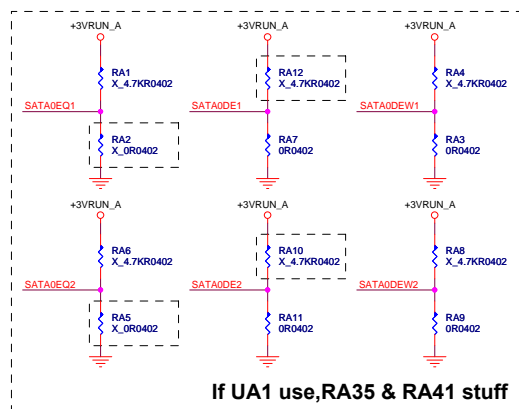
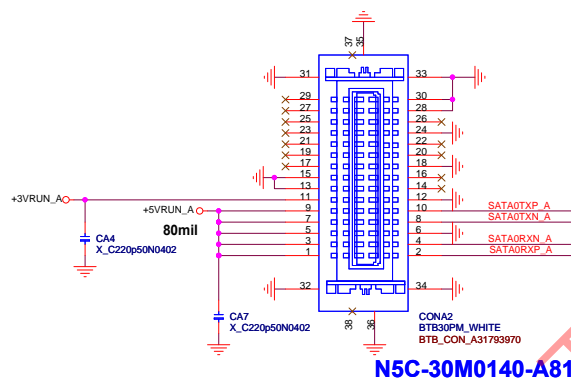
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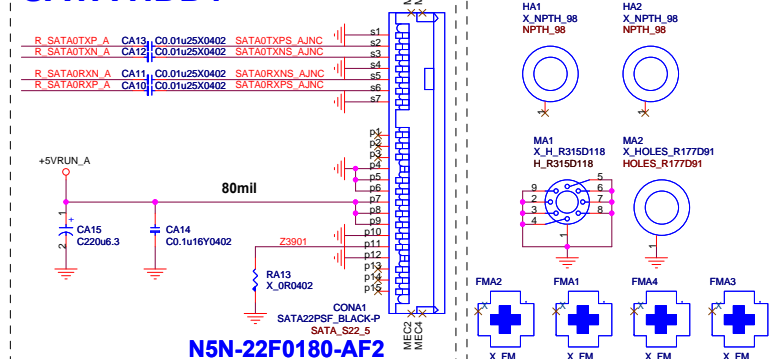
Screw



BTB Conn From Port 3



SATA HDD1



TI SN75LVCP601RTJR HW Setting

EQ1/EQ2	CH1/CH2Equalization dB (@6Gbps)	DE1/DE2	CH1/CH2De-Emphasis dB(@6Gbps)
NC (default)	0	NC (default)	-6
0	7	0	0
1	14	1	3

DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (default)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)

MS-1763A Change List

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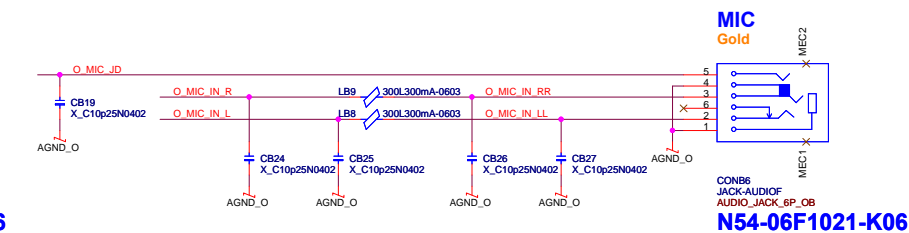
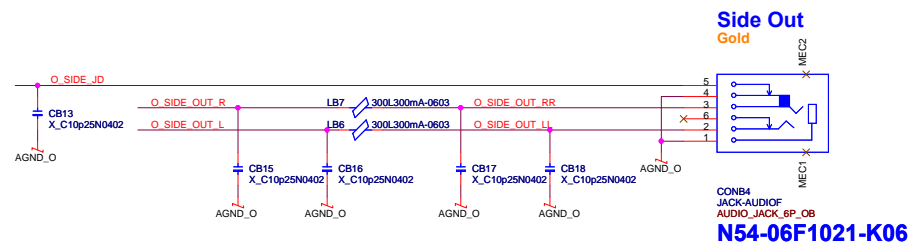
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Date	Page	Description

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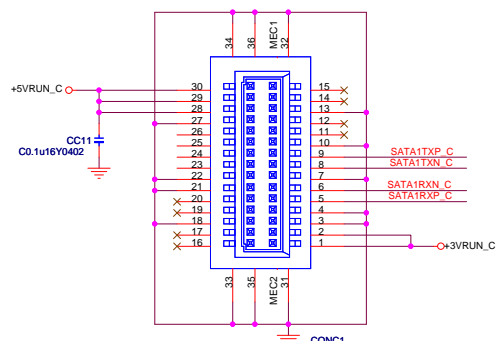
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Title	HDD1
Size	Document Number
	MS-1763A
Date:	Thursday, March 21, 2013
Sheet	34 of 44

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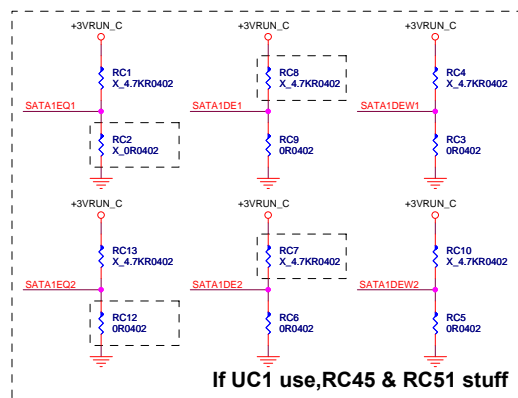


MS-1763B Change List					
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			<div> <div>msi</div> <div>MICRO-STAR INT'L CO.,LTD.</div> </div> <div> <div>Title</div> <div>IO/Audio Board</div> </div> <div> <div>Size</div> <div>Document Number</div> <div>MS-1763B</div> </div> <div> <div>Date</div> <div>Thursday, March 21, 2013</div> <div>Sheet</div> <div>35</div> <div>of</div> <div>44</div> </div> <div> <div>Rev</div> <div>1.</div> </div>		

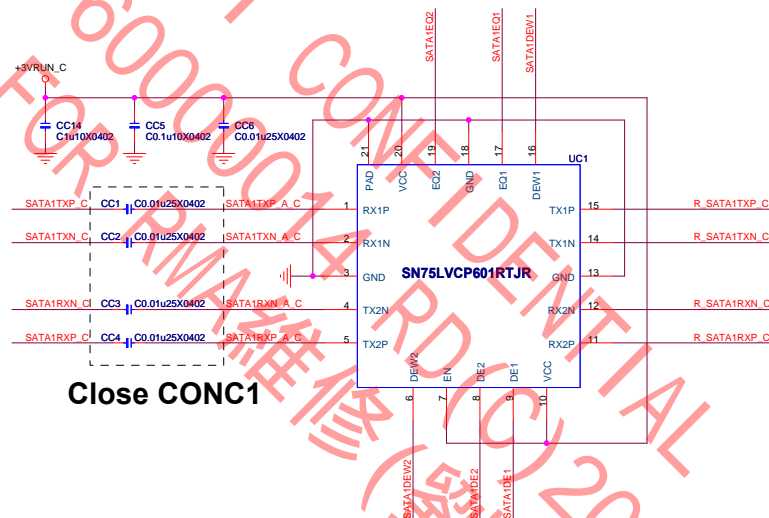
BTB Conn From Port 1



N5C-30M0170-A81

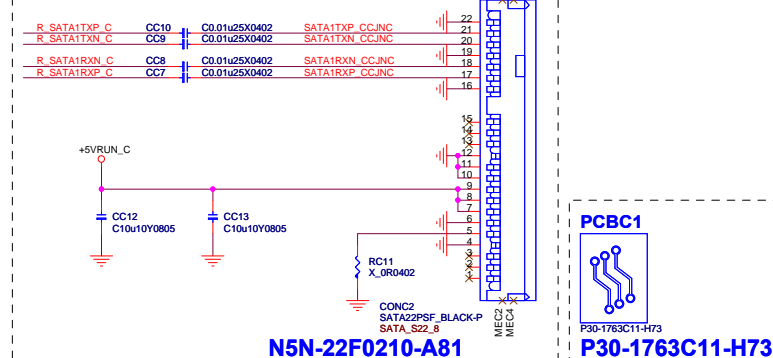


If UC1 use RC45 & RC51 stuff



Close CONC1

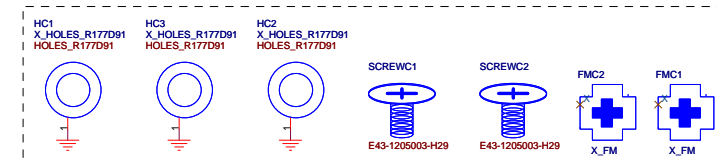
SATA Conn



N5N-22F0210-A81

PCBC1

P30-1763C11-H73



TI SN75LVCP601RTJR HW Setting

EQ1/EQ2	CH1/CH2Equalization dB (@6Gbps)	DE1/DE2	CH1/CH2De-Emphasis dB (@6Gbps)
NC (default)	0	NC (default)	-6
0	7	0	0
1	14	1	-3

DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (default)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)

MS-1763C Change List

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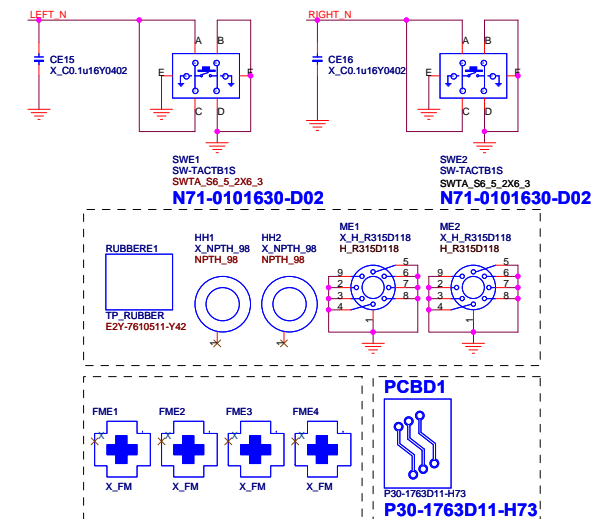
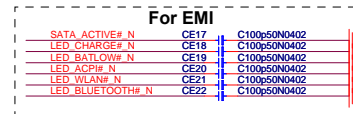
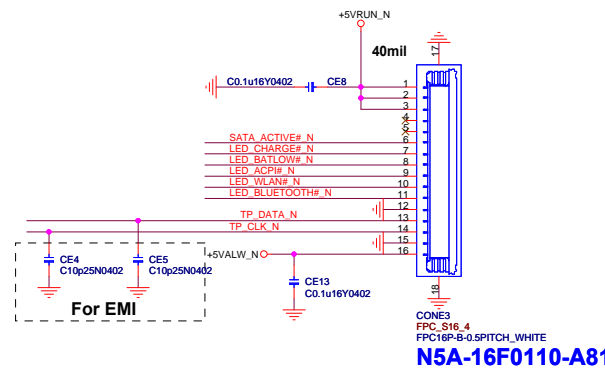
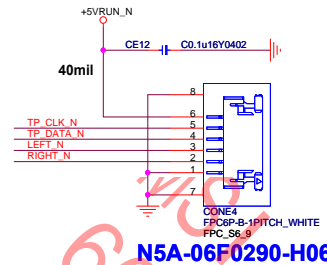
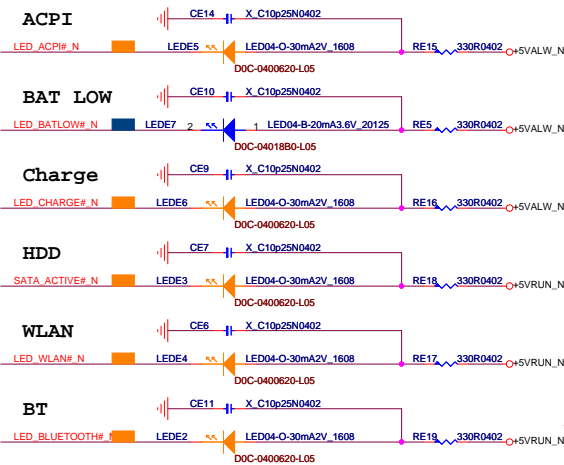
MICRO-STAR INT'L CO.,LTD.

HDD2
MS-1763C

Rev 1.1

Date: Friday, March 22, 2013

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Date	Page	Description
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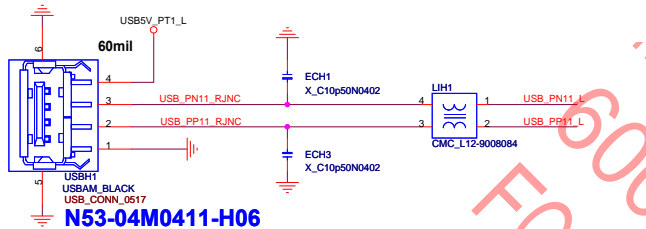
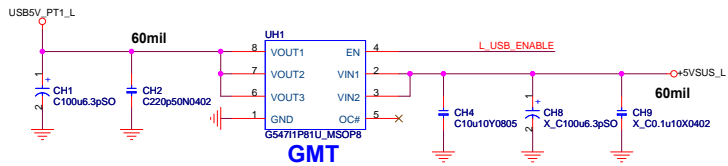
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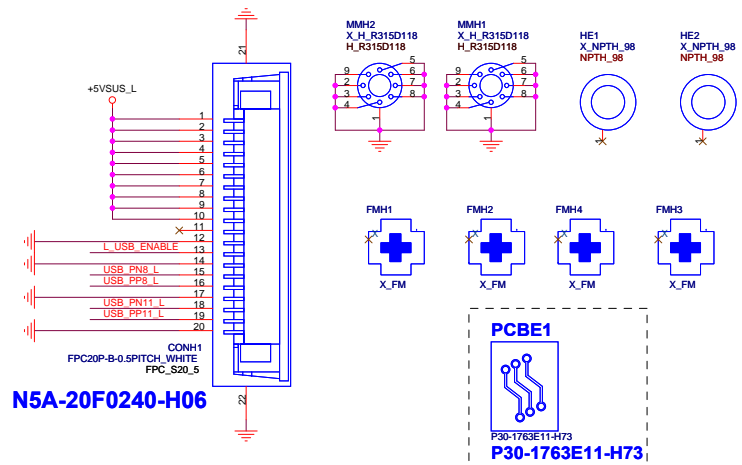
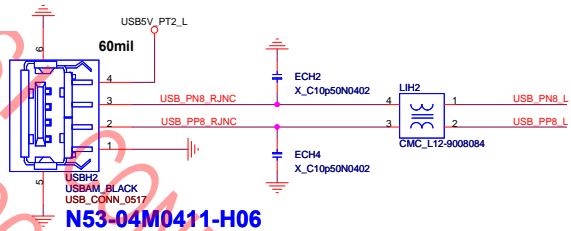
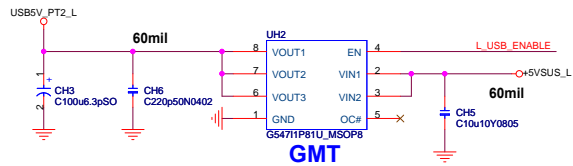
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07

USB4



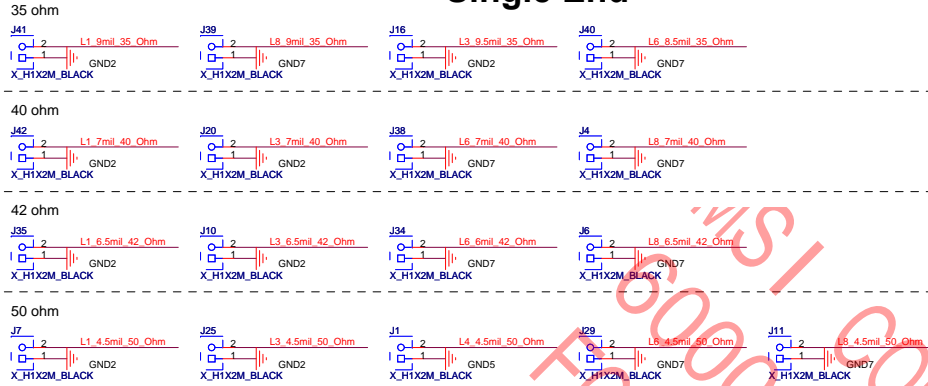
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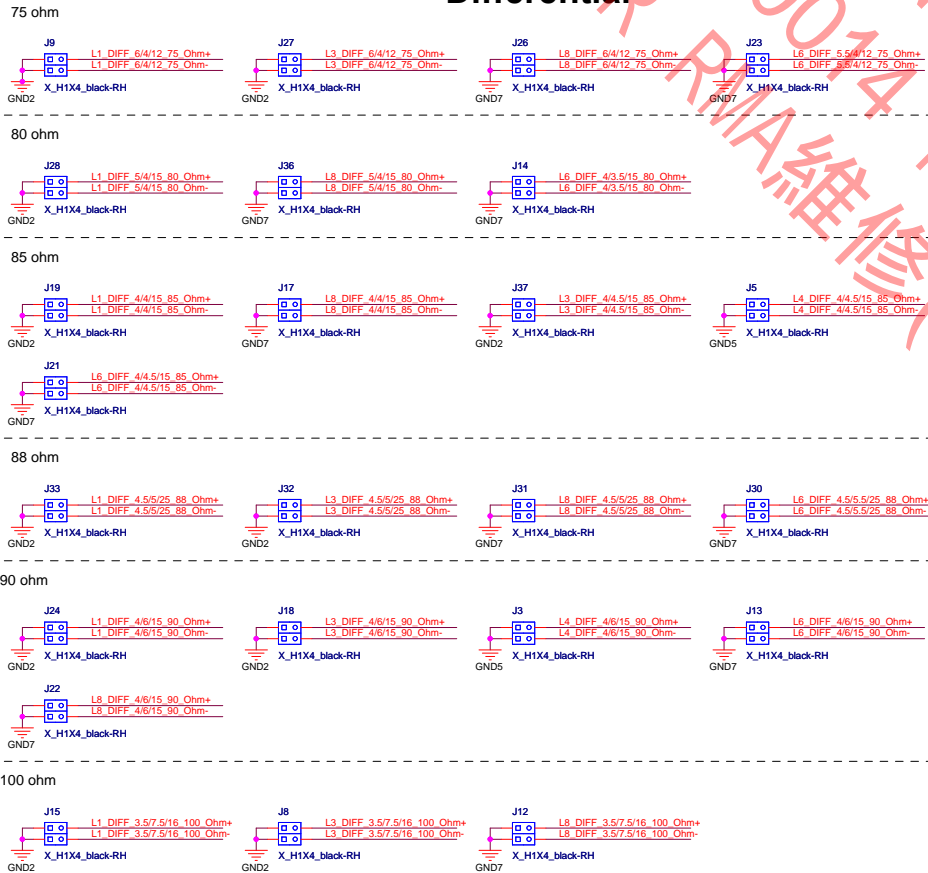
MS-1763E Change List

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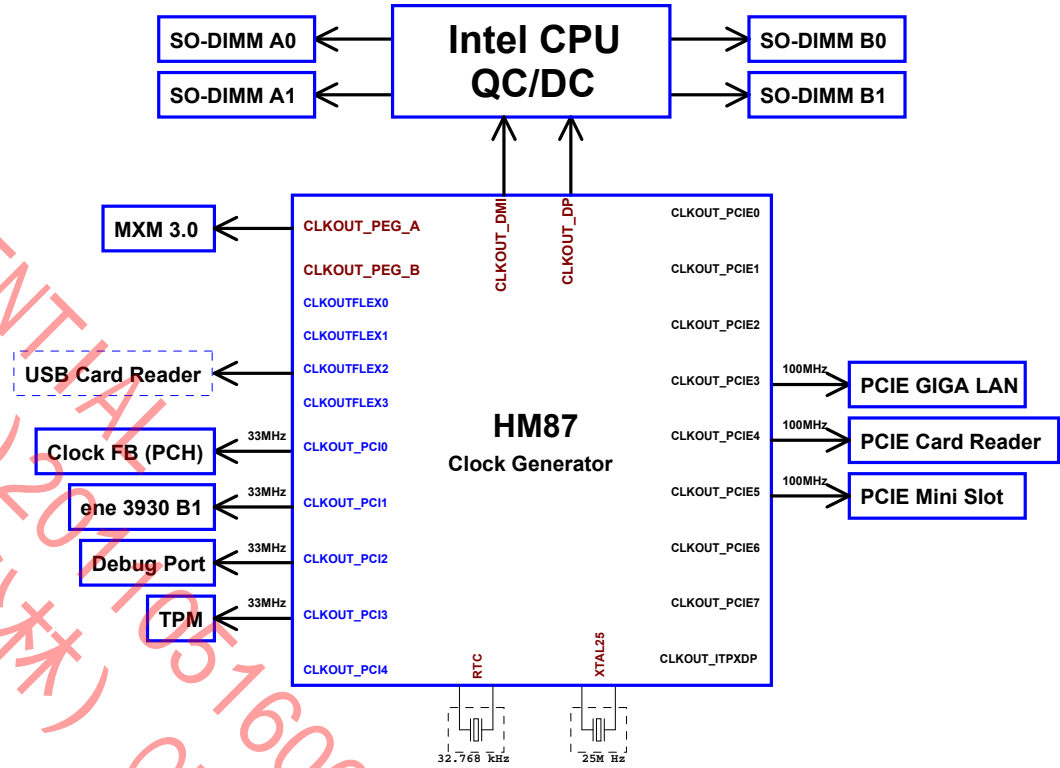


Differential



Clock Distribution

Internal Clock Mode



Power on Sequence

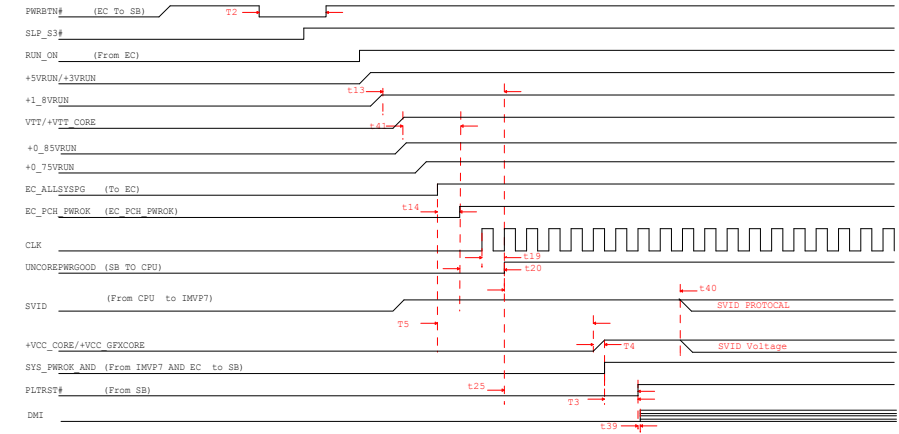
S5-S0

EC programming timing



S3-S0

EC programming timing

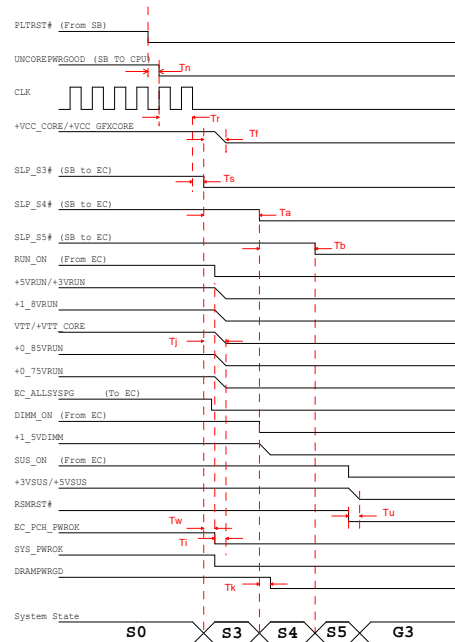


	Min	Max	Unit	Description
T1	150		mS	
T2	16		mS	
T3	1		mS	Timing set by PCH
t04	10		mS	
t07	100		mS	
t08		90	mS	
t09	30		uS	
t10	30		uS	
t13	5	650	mS	
t14	99		mS	EC Delay
t17	2	650	mS	
t18	1		mS	Timing set by PCH
t19	41		mS	Timing set by PCH
t20	2		mS	Timing set by PCH
t25	1	100	mS	
T5		800	uS	Follow MVP Spec
T4	2.5		mV/uS	Follow MVP Spec
t39		200	uS	
t40		500	uS	
t41	10		mS	

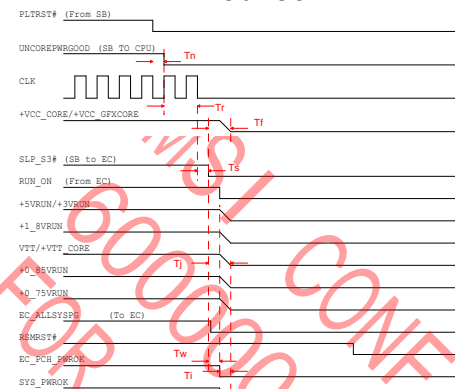
Power down Sequence

S0-S5

EC programming timing

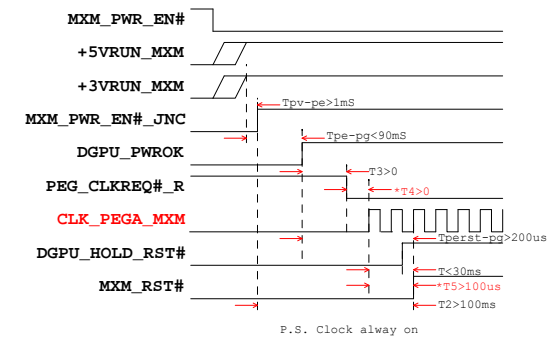


S0-S3

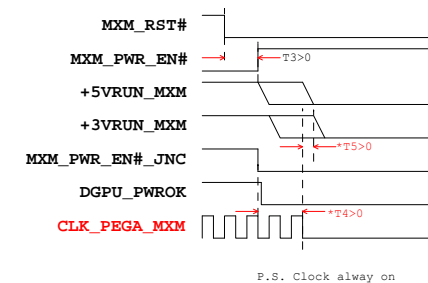


	Min	Max	Unit	Description
Ta	30		uS	
Tb	30		uS	
Tf		500	mS	
Ti	40		nS	
Tj	5		uS	
Tk	100		nS	
Tn	30		uS	
Tp	500		uS	Sx-RSMRST#
Tr	10		uS	
Ts	1		uS	
Tu	40		nS	
Tw	0		mS	

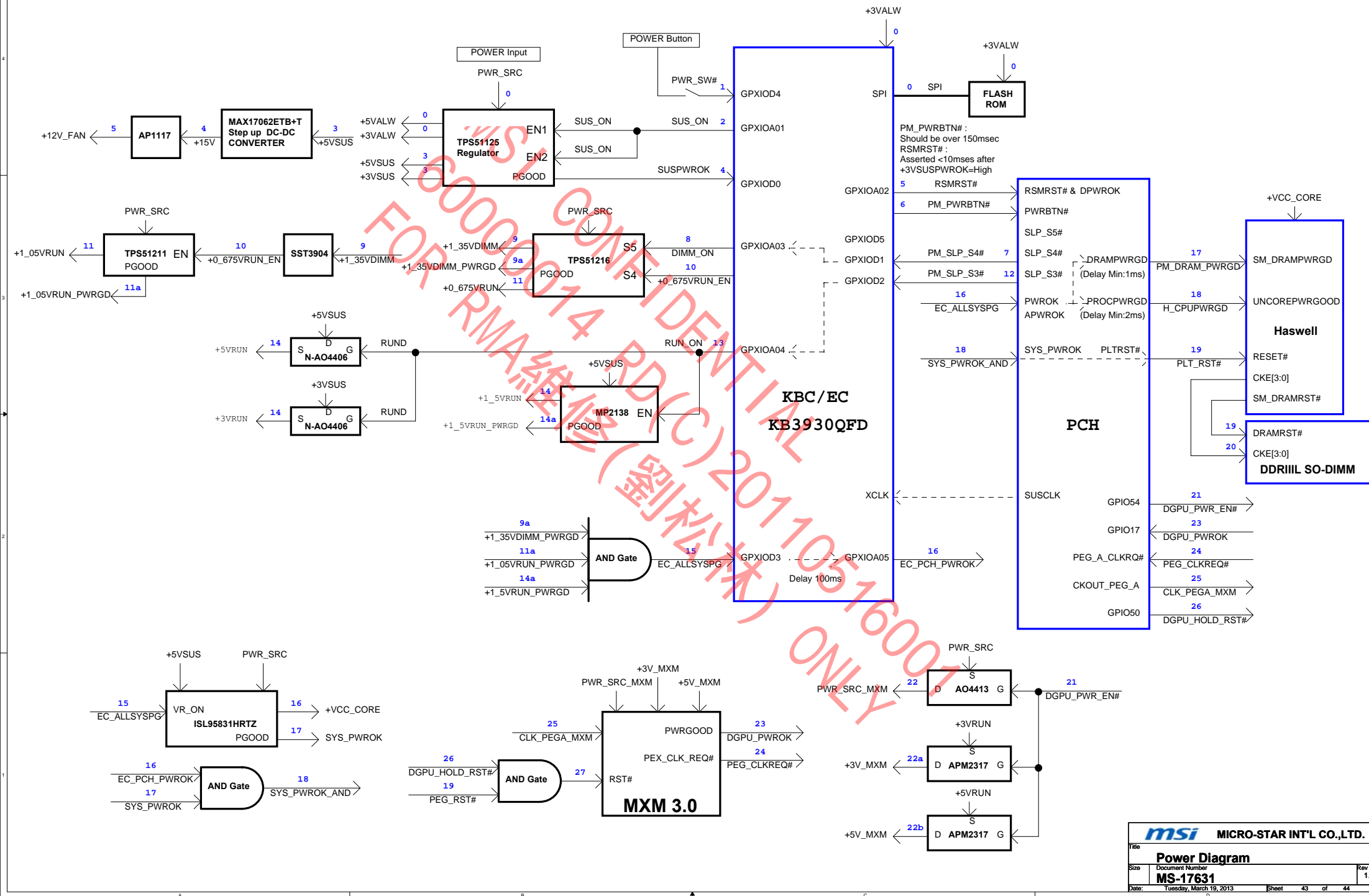
Power-Up Sequence For Optimus On MXM



Power-Down Sequence For Optimus On MXM



Power Diagram



DC_IN
Adaptor 180W

BQ24737
Charger

ISL95812HRZ
+VCC_CORE

N MOS
SM4370N

+VCC_CORE / 85A

N MOS
SM4373N

TPS51216RUKR
+1.35VDIMM

N MOS
SM4370N

+1.35VDIMM / 16.2A

N MOS
SM4373N

+0.675VRUN / 2A

TPS51211DSCR
+1.05V

N MOS
SM3316N

+1.05VRUN / 6.68A

N MOS
SM3316N

TPS51125RGER
+3VALW/+5VALW

N MOS
SI4914BDY

+3VSUS / 9.586A

N MOS
AO4406AL

+3VRUN / 7.733A

N MOS
SM4370N

+5VSUS / 21.2A

N MOS
AO4406AL

+5VRUN / 6.5A

N MOS
SM4373N

+3VALW / 20mA

KB3930QFB1	
VCC	3.3VALW 20mA

MAX17062ETB+T
+15V

AP1117
+12V

MP2138DQT
+1.5VRUN

+1.5VRUN / 624mA

Power Name	Current
VCC_CORE	85A
1.35VDIMM	16.2A
0.675VRUN	2A
1.05VRUN	6.68A
3VSUS	6.886A
3VRUN	5.033A

Power Name	Current
5VSUS	21.22A
5VRUN	6.5A
15V	2.16A
12V	2.7A
1.5VRUN	624mA
3VALW	20mA

MXM 3.1	
PWR_SRC	19V 10A
3.3V	3VRUN 1A
5V	5VRUN 2.5A

ANX1122	
3.3V	3VRUN 0.081mA
1.05V	1.05VRUN 0.11mA

TPM	
VS	3VSUS 25mA
VDD	3VRUN 5mA

Camera	
VCC	3VRUN 350mA

MCU	
VCC	3VRUN 25mA

P2501	
VCC	3VRUN 25mA

Haswell (rPGA 947)	
VCC_CORE	1.2V 85A
VDDQ	1.35V 4.2A
Lynx Point HM87	
VCC3_3	3.3V 223mA
VCCIO	1.05V 6.67A
VCCVRM	1.5V 179mA
VCCDSW	3.3V 286mA
VCCADAC	1.5V 70mA
DDR 3L	
VDDQ	1.35VDIMM 12A
VREF	0.675VRUN 2A
LVDS	
VDD	3.3VRUN 2A
VLED	19V 1.5A
Realtek RTS5209	
3V3_IN	3VRUN 300mA
CPU FAN	
VCC	12V 2.7A
ALC892-CG	
VDD33	3VSUS 1mA
AVDD	5VSUS 60mA
DVDD	3VSUS 41mA
Amplifier	
VDD	5VSUS 485mA
HVDD	3VRUN 5mA
Mini PCI-E	
+3.3V	3VRUN 1.1A
+1.5V	1.5VRUN 375mA
USB Ports	
USB 2.0*2	5VSUS 1.5A
USB 3.0*3	5VSUS 6A
Bigfoot E2200	
VDD33	3VSUS 1.5A
SATA Ports	
HDD	5VRUN 2A
ODD	5VRUN 2A
mSATA	3VRUN 2.7A